International Journal of Sciences and Techniques of Automatic control & computer engineering
IJ-STA, Special Issue, CEM, December 2008, pp. 590–601.

Carrier overlapping PWM methods for single phase cascaded five level inverter

B. Shanthi* and S. P. Natarajan**

**Centralised Instrumentation and Service Laboratory, Annamalai University,*
Email: au_shan@yahoo.com
***Department of Instrumentation Engineering, Annamalai University,*
Email: spn_annamalai@rediffmail.com

Abstract. *A single phase cascaded inverter consisting of two full bridges creates a five level AC output voltage. Due to switch combination redundancies, there are certain degrees of freedom to generate the five level AC output voltage. This paper presents the use of Control Freedom Degree (CFD) combination. The effectiveness of the Pulse Width Modulation (PWM) strategies developed using CFD are demonstrated by simulation. The simulation results indicate that the use of CFD combination is an important clue to realize high performance multilevel inverter and the COPWM-A strategy developed exhibits reduced harmonics for moderate modulation indices and higher DC bus utilization than non-overlapping PWM methods. PWM strategies developed are implemented in real time using dSPACE/Real Time Interface (RTI). The simulation and experimental results closely match with each other validating the strategies presented.*

Keywords. *Multilevel inverters, PWM, CFD, dSPACE.*

1. Introduction

Multilevel inverter has drawn tremendous interest in high power applications because it has many advantages: it can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. When the number of output levels increases, harmonics of the output voltage and current as well as Electro Magnetic Interference (EMI) decrease. Three PWM methods with different vertical and horizontal offset combinations are investigated in [1-3] leading to the quantification of their output harmonics. Multilevel PWM methods based on control degrees of freedom combination and their theoretical analysis are discussed in [4].

Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load. Fig.1 shows a single phase 5-level configuration of the Modular Structured Multilevel Inverter

This paper was recommended for publication in revised form by the editor Staff.
Edition: CPU of Tunis, Tunisia, ISSN: 1737-7749

(MSMI). The MSMI is unique when compared to other types of multilevel inverters in the sense that it consists of several modules that require separate DC sources.

Compared to other types of multilevel inverters, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation. As can be seen from Fig. 1, each module of the MSMI has the same structure whereby it is represented by a single phase full-bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging.

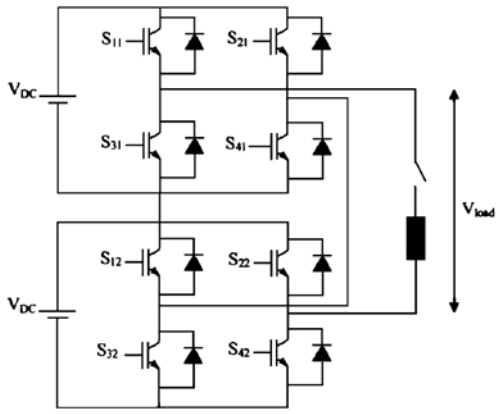

Fig.1. Five Level MSMI

The operation of the MSMI can be easily understood whereby the load voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (M) which is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the MSMI. It is usually assumed that m is odd as this would give an integer valued M which would simplify further analysis. In this work, load voltage consists of five levels which include $+2V_{DC}$, $+ V_{DC}$, 0, $- V_{DC}$ and $-2V_{DC}$ and the number of modules needed is 2. The following equation gives the relationship between M and m.

$$M=(m-1)/2$$

The gate signals for chosen five level cascaded inverter are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter. The PWM strategies developed are implemented in real time using dSPACE/RTI for only one value of modulation index (0.8). The simulation and experimental results are compared and evaluated.

2. Modulation strategies for multilevel inverter

A number of modulation strategies are used in multilevel power conversion applications. They can generally be classified into three categories:

- Multistep, staircase or fundamental frequency switching strategies
- Space Vector PWM strategies
- Carrier based PWM strategies

Of all the PWM methods for cascaded multilevel inverter, carrier based PWM methods and space vector methods are often used but when the number of output level is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM method is preferred under this condition in multilevel inverters. This paper focuses on carrier based PWM techniques which have been extended for use in multilevel inverter topologies by using multiple carriers.

Multilevel carrier based PWM methods have more than one carrier that can be triangular waves or sawtooth waves and so on. As far as the particular carrier signals are concerned, there are multiple CFD including frequency, amplitude, phase of each carrier and offsets between carriers. The modulating/ reference wave of multilevel carrier based PWM method can be sinusoidal or trapezoidal. As far as the particular reference wave is concerned, there is also multiple CFD including frequency, amplitude, phase angle of the reference wave and as in three phase circuits, the injected zero sequence signal to the reference wave. Therefore, multilevel carrier based PWM methods can offer multiple CFD. These CFD combinations combined with the basic topology of multilevel inverters can produce many multilevel carrier based PWM methods.

3. Carrier based PWM methods based on CFD combination

This paper presents three Carrier Overlapping PWM (COPWM) methods that utilize the CFD of vertical offsets among carriers. They are: COPWM-A, COPWM-B, COPWM-C. The above three methods are simulated. For comparison purposes, a non-overlapping Sub-Harmonic PWM (SHPWM) method is also presented in this work.

For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude of A_m and frequency of f_m and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off. The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method as follows:

$$m_a = A_m/((m/4)* A_c) \qquad m_f = f_c / f_m$$

In this paper, m_f =21, A_c=1.6 and m_a is varied from 0.5 to 0.9.

3.1 SHPWM method

The principle of the SHPWM method is to use several triangular carriers with only one modulation wave. For an m-level inverter, m-l triangular carriers of the same frequency f_c and the same peak-to-peak amplitude A_c are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. Carrier arrangement for 5-level SHPWM are shown in Fig.2.

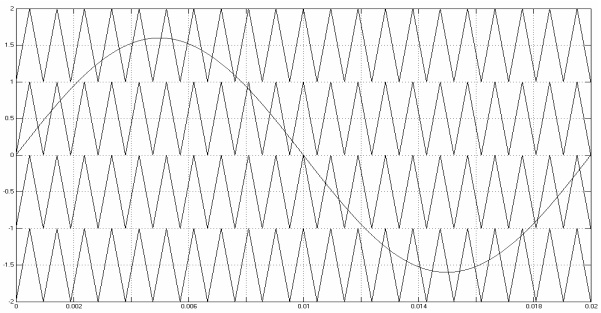

Fig. 2. Carrier arrangement for SHPWM method (m_a=0.8)

3.2 COPWM-A method

The vertical offset of carriers for 5-level inverter with COPWM-A method is illustrated in Fig.3. It can be seen that the four carriers are overlapped with other and the reference sine wave is placed at the middle of the four carriers.

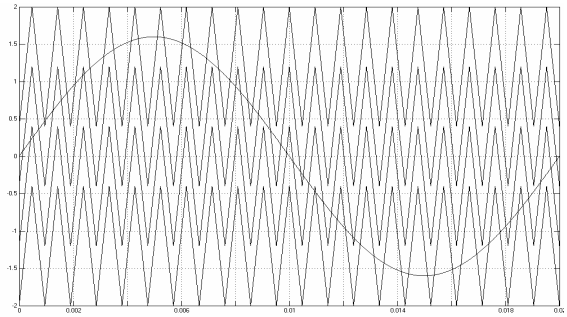

Fig. 3. Carrier arrangement for COPWM-A method(m_a=0.8)

3.3 COPWM-B method

Carriers for 5-level inverter with COPWM-B method are shown in Fig.4. It can be seen that they are divided equally into two groups according to the positive/negative average levels. In this type the two groups are opposite in phase with each other while keeping in phase within the group.

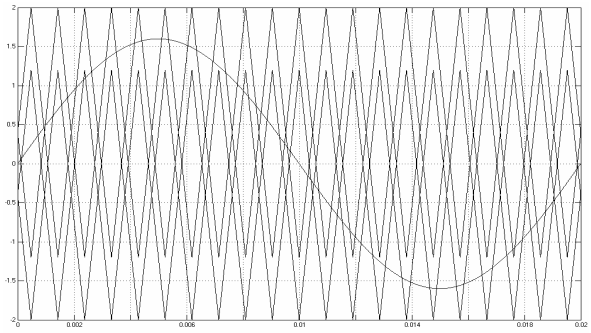

Fig. 4. Carrier arrangement for COPWM-B method (m_a=0.8)

3.4 COPWM-C method

Carriers for 5-level inverter with COPWM-C method are shown in Fig.5. In this pattern, the carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude-overlapped and neighbouring-phase-interleaved carriers. Actually, pattern B and C have second control freedom change with the carriers' horizontally phase shifted from pattern A besides the offsets in vertical.

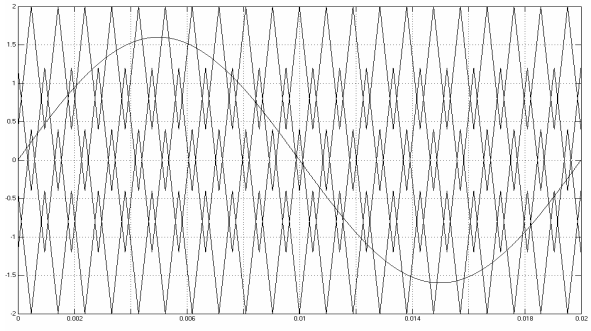

Fig. 5. Carrier arrangement for COPWM-C method (m_a=0.8)

4. Simulation results

The cascaded 5-level inverter is modelled in SIMULINK using Power system

block set. Switching signals for cascaded multilevel inverter using SHPWM and COPWM techniques are also simulated.

Simulations are performed for different values of m_a ranging from 0.5 – 0.9 and the corresponding %THD are measured using the FFT block and their values are shown in Table I. Next table displays the V_{rms} of inverter output for different modulation indices. Figs. 6 – 13 show the simulated output of MSMI inverter with above strategies but for only one sample value of $m_a = 0.8$.

Fig.6 shows the five level output voltage generated by SHPWM switching strategy and its FFT plot is shown in Fig.7. Fig.8 displays the five level output voltage generated by COPWM-A switching strategy and its FFT plot is shown in Fig.9. Fig.10 shows the five level output voltage generated by COPWM-B switching strategy and its FFT plot is shown in Fig.11. Fig.12 shows the five level output voltage generated by COPWM-C switching strategy and its FFT plot is shown in Fig.13. Fig.14 shows a graphical comparison of %THD in various strategies for different modulation indices. The following parameter values are used for simulation: V_{DC} =100V, A_c=1.6, m_f=21 and R(load) = 50 ohms.

5. Experimental results

This section presents the results of experimental work carried out on chosen MSMI using a dSPACE DS1104 controller board which is based on the Texas Instruments TMS320F240 floating-point DSP. Real time implementation of these strategies using MATLAB – dSPACE/RTI requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/ SIMULINK.

The dSPACE system is an embedded or self contained system. The dSPACE system combines a data acquisition system with an independent processing system to implement digital control. It is specifically designed for the development of high-speed multivariable digital controllers. It is a real time control system based on a 603 power PC floating-point processor with four multiplexed inputs to 16-bit Analog to Digital Converter (ADC), four inputs with independent 12-bit ADCs and an 8 - output digital to analog converter running at 250 MHz. For advanced I/O purposes, the board includes a slave-DSP subsystem based on the TMS320F240 DSP.

The dSPACE system can be plugged into a PCI slot of a PC. The gate signal generation block using different PWM strategies listed above is designed and developed using SIMULINK and downloaded to dSPACE / RTI. The results of the experimental study are shown in the form of the PWM outputs of chosen MSMI.

Optocoupler circuit provides isolation between the control circuit and the power converter circuit. The optocoupler used is 6N137, which is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is inversion of the applied input. The PWM signals from the dSPACE are not capable of driving the MOSFETs. In order to strengthen the pulses a driver circuit is provided.

Fig.15-18 show the experimental output voltage of the single phase cascaded 5-level inverter obtained using dSPACE/RTI with strategies SHPWM, COPWM-A, COPWM-B and COPWM-C respectively.

Fig.19 shows the entire hardware setup. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 40V.

6. Conclusion

In this paper, CFD based PWM strategies for chosen MSMI have been presented. The COPWM-A method provides lower THD than the other methods for moderate m_a whereas for high m_a (0.9), the SHPWM method provides better performance (Table I). COPWM method provides high DC bus utilization as in Table II.

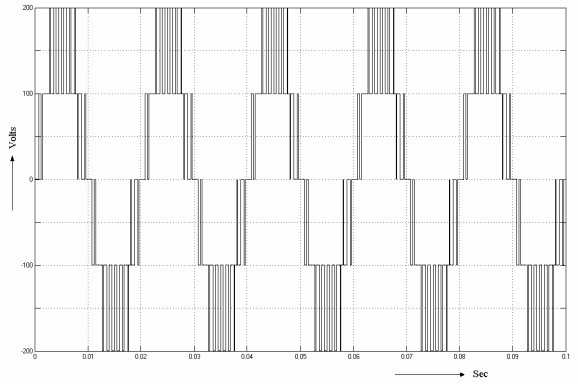

Fig. 6. Output voltage generated by SHPWM method

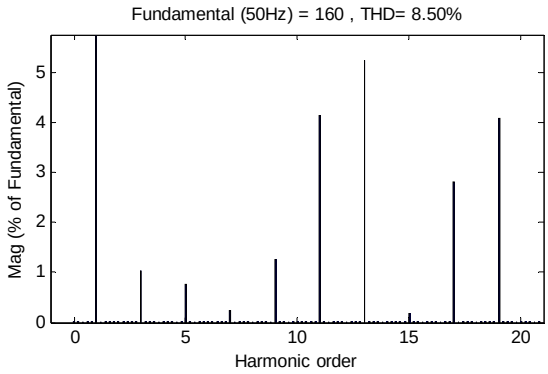

Fig. 7. FFT plot for SHPWM method

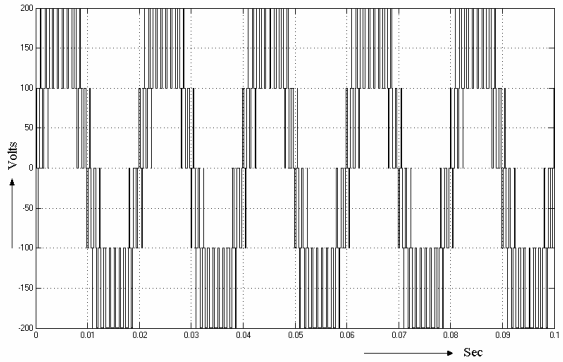

Fig. 8. Output voltage generated by COPWM-A method

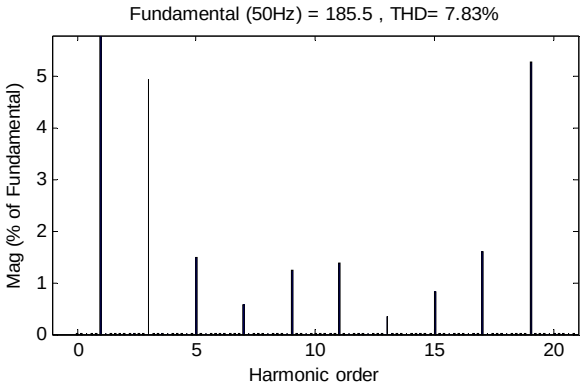

Fig. 9. FFT plot for COPWM-A method

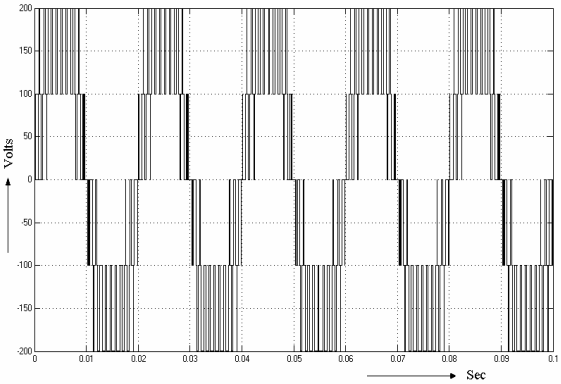

Fig. 10. Output voltage generated by COPWM-B method

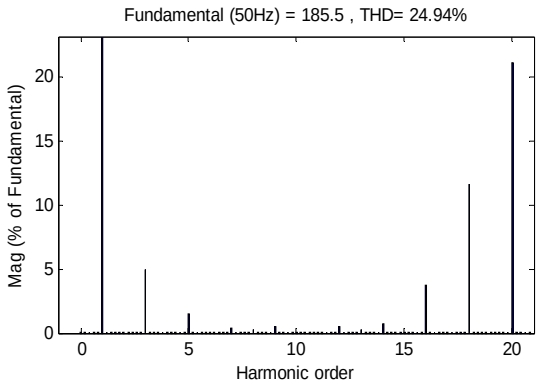

Fig. 11. FFT plot for COPWM-B method

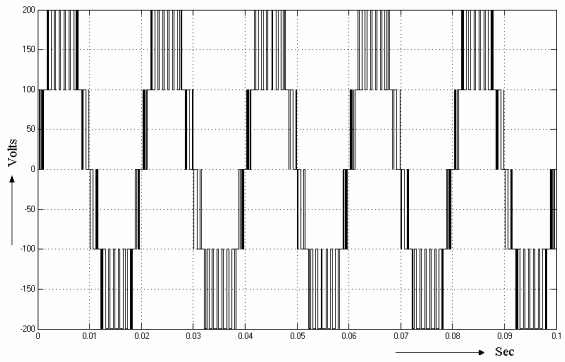

Fig. 12. Output voltage generated by COPWM-C method

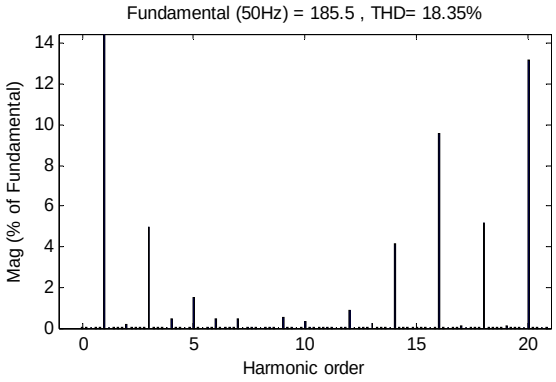

Fig. 13. FFT plot for COPWM-C method

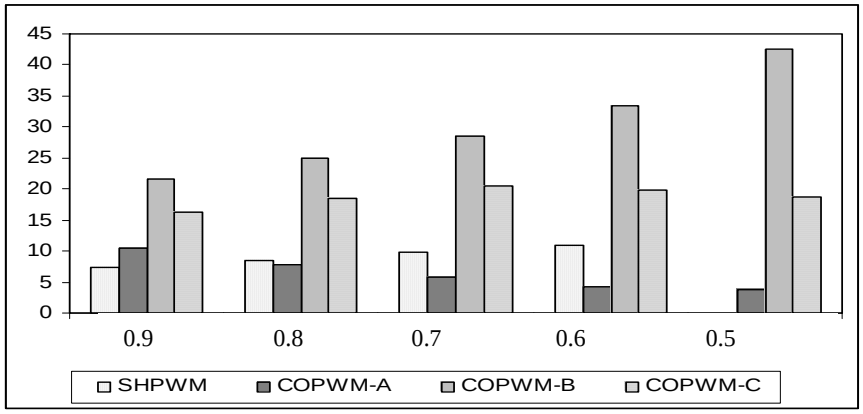

Fig.14. %THD Vs m_a

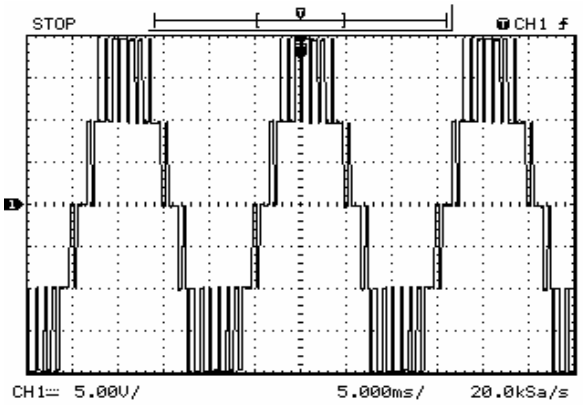

Fig.15. Output voltage of cascaded five level inverter using SHPWM method

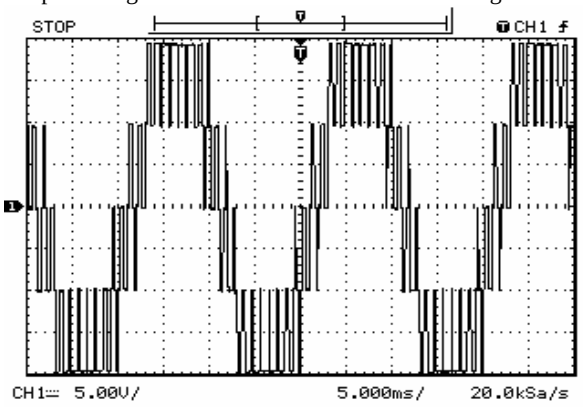

Fig.16. Output voltage of cascaded five level inverter using COPWM-A method

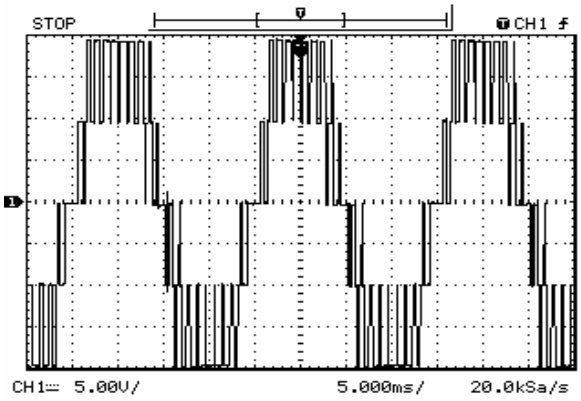

Fig.17. Output voltage of cascaded five level inverter using COPWM-B method

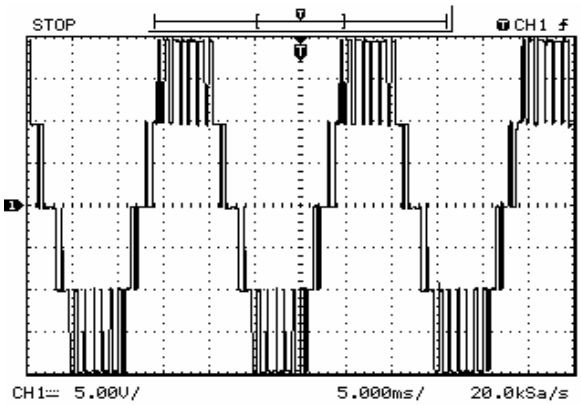

Fig.18. Output voltage of cascaded five level inverter using COPWM-C method

Fig.19. Hardware setup of five level MSMI

Table 1. %THD for different modulation indices

m_a	%THD			
	SHPWM	COPWM-A	COPWM-B	COPWM-C
0.9	7.35	10.39	21.7	16.2
0.8	8.5	7.83	24.94	18.35
0.7	9.7	5.72	28.6	20.6
0.6	11	4.28	33.4	19.9
0.5	--	3.73	42.5	18.7

Table 2. RMS output voltage for different modulation indices

m_a	V_{rms} in volts	
	SHPWM	COPWM
0.9	127.3	141.7
0.8	113.1	131.2
0.7	98.98	119.8
0.6	84.84	106.9
0.5	--	88.36

7. References

1. A. Nabae, I. Takahashi and H. Akagi: A new neutral-point clamped PWM inverter, IEEE Trans. Ind. Applicat., Vol. IA-17, Sept/Oct.(1981) 518-523.
2. J. S. Lai and F. Z. Peng: Multilevel converters-A new breed of power converters, IEEE Trans. Ind. Applicat., Vol. 32, May/June (1996) 509-517.
3. G. Carrara, S. Gardella, M. Marchesoni, R. Salutari and G. Sciutto: A new multilevel PWM method: A theoretical analysis, IEEE Trans.Power Electron, Vol. 7, July (1992) 497–505.
4. Yan Deng, Hongyan Wang, Chao Zhang, Lei Hu and Xiangning He: Multilevel PWM methods based on control degrees of freedom combination and its theoretical analysis, IEEE IAS 2005 Conference Record no.: 0-7803-9208-6/05, 1692 – 1699.