Reduce Harmonics in Three Level NPC Shunt Active Power Filter Using Fuzzy Logic and Hysteresis Current Control

Habiba Bellatreche , Abdelhalim Tlemçani

***Abstract*—Non-linear loads inject harmonics into electric power systems distribution network, which deteriorate power quality and pollute the entire power system. Shunt Active Power Filters (APF) are considered as the dynamic solution for mitigation harmonics, compensate reactive power and balance supply loads. In this paper research, using synchronous reference frame (SRF) algorithm as an extraction harmonic method, a three phase three level shunt APF is developed under ideal source voltage conditions. A novel approach based on variable band hysteresis current control is proposed and Fuzzy Logic Controller (FLC) has been applied successfully to keep the dc-link capacitor voltage constant. The performance of the proposed scheme is evaluated in terms of current source compensation, reduction in total harmonic distortion as per IEEE-519 standard. All simulation results are discussed in Matlab/Simulink environment.**

***Index Terms*—Shunt Active Power Filter, Synchronous Reference Frame; Neutral Point Clamped, Fuzzy Logic Controller, Hysteresis Current Control, Total Harmonic Distortion.**

NOMENCLATURE

i_{La} , i_{Lb}, i_{Lc}	Actual load currents
i_a^*, i_b^*, i_c^*	Instantaneous reference currents
i_α , i_β	Stationary reference frame currents
$i_{\alpha h}$, $i_{\beta h}$	Harmonic stationary reference frame currents
i_d , i_q	Rotating reference frame grid currents
$\overline{i_d}$, $\overline{i_d}$	Mean value rotating reference frame currents
$\tilde{i_d}$, $\tilde{i_q}$	Alternative rotating reference frame currents
I_{max}	Magnitude of peak reference grid currents
ΔI	Current hysteresis band
X	Discourse universe

I. INTRODUCTION

Power systems include different nonlinear loads. Static power converters, saturated magnetic devices, rotating machines used in industry and other electronics equipments change the sinusoidal nature of the AC power current (consequently the AC voltage drop). This problem results in power factor, degradation and generates alternating voltages and currents have a different frequency than the fundamental [1].

Harmonics problem in power system can be rectified by involving passive filters in the grid combined with an inductor and a capacitor [2] connected in shunt with the load. Though passive filter impedance is a problem; at a tuned harmonic frequency, filter exhibits lower impedance than the source [3], hence, it bypasses major part of the harmonic currents to diminish the harmonic currents flowing into the source. Other inherent problems, which discourage the use of this method, are that has the limitations of fixed compensation, larger component size, and can also, excite resonance conditions.

Active power filter (APF) is an alternative effective solution to filter harmonics [4]. Its principle is based on injection of a compensating current in opposite polarity to the harmonic currents produced by nonlinear load [5] in order to have a sinusoidal waveform of voltage and current in network and sometimes rendered with a unity power factor.

APF is widely used in power network [6], it performance depends on technique used to determine reference current estimation, method chosen to control switches of inverter and conception of DC voltage control loops. In this paper author discussed all these points using an APF composed of an inverter based on three-level Neural Point Clamp topology (3L-NPC) and associated with fuzzy logic controller (FLC) which has generated an immense interest results and good effects in filter.

Nowadays, three commercial topologies of multilevel inverters exist [7]: NPC, fling capacitors (FCs), and cascaded H-bridge (CHB). NPC inverter was presented in 1980 by Nabae [8], author invests in advantages of 3L-NPC topology such as reduced switching losses, smaller output current ripple, and total supply voltage is split. Only half of the voltage has to be switched, and this also cuts the switching losses in the transistor by half. The DC voltage is divided into a positive and negative voltage, which supports the serial connection of DC capacitors without the need for leakage current compensation [9].

Keep constant the DC capacitor voltage is one of the significant tasks in shunt APF [10]. This is essential because

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there is energy loss due to conduction and switching power losses associated with the controllable switches of the inverter, which tend to diminish the value of DC capacitor voltage. Conventional regulator (PID) requires an accurate mathematical model which is hard to obtain. Therefore author has selected a FLC; it is based on a linguistic description, needed very less tuning efforts as it has intelligent mapping between input and output, which is linguistic rather than mathematical [11].

The background presented in current paper is divided into five main sections. Topological overview of shunt APF includes 3L-NPC converter is presented at first, then it can see in second section the synchronous reference frame approach which is developed to extracts harmonic in APF design. After 3L-NPC inverter is discussed. In section IV, variable band hysteresis current control is treated. Finally FLC is chosen to regulate the DC side capacitor voltage. All simulation results are described and discussed.

II. SHUNT ACTIVE POWER CONFIGURATION

Shunt APF is the most important configuration used in active filtering application for current harmonic reduction and power factor improvement. It operates as injecting current harmonic source, consequently it has the capability to inject equal and opposite harmonics current onto the power system.

The parallel filters have advantages such as: small size , tuning is easy and accurate ,elimination of harmonics currents, compensating reactive power, correction of power factor and rebalancing currents of nonlinear load [12]. Fig.1 illustrates a typical shunt APF and Fig.2 the non-linear load.

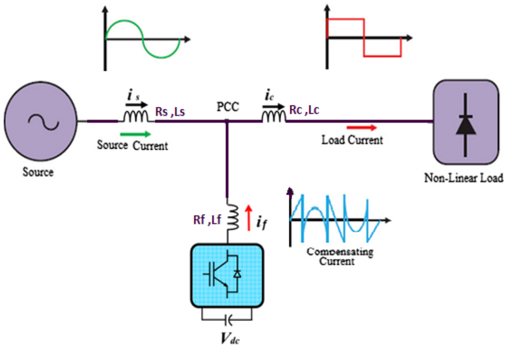


Fig. 1. Basic configuration of shunt APF.

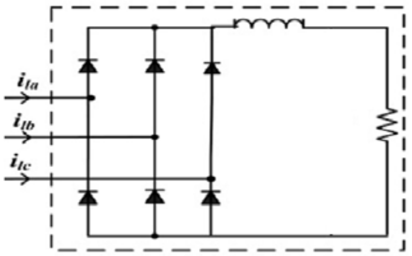


Fig. 2. Three phase non-linear load.

III. REFERENCE CURRENT GENERATION

The APF control strategy determines the reference signals (current and voltage) and thus, decides the switching instants of inverter switches, such that the desired performance can be achieved. Several harmonic current identification methods have been investigated by many researchers such as synchronous detection, average mode, instantaneous active and reactive powers method [13]. The main task of harmonic currents compensation is to determine the harmonic current references to be generated by the active filter, after it controlled to generate the identified harmonic currents and inject them in the main electrical power grid.

Synchronous Reference Frame (SRF) is one of popular methods harmonic component extraction. This theory is extensively used as it simplicity of the algebraic calculations. In this method, the load current at the point of common coupling (PCC) is measured then has already been transformed from (abc) stationary coordinate to (dq-0) rotating coordinate system transformation [14]. It is done using following equations.

First, identified and transformed into stationary two-phase frame (αβ-0) from the three-phase stationary frame (abc), as per (1).

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} \tag{1}$$

After, the two phase current quantities i_α and i_β of stationary (αβ-0) axes are transformed into two-phase rotating synchronous frame (dq-0) using (2). Phase Locked Loop circuit (PLL) is providing cos (θ) and sin (θ) which represents the synchronous unit vectors for transformation of the supply current source.

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix}\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \tag{2}$$

Equation (2) contains AC component or oscillating value as well as DC component or average value, see (3).

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \bar{i_d} + \tilde{i_d} \\ \bar{i_q} + \tilde{i_q} \end{pmatrix} \tag{3}$$

To eliminate the AC component which contain harmonic component, low pass filter is used. So that DC component which is output of above equation is harmonic free. Next, this harmonic free signal in (dq-0) rotating frame is converted back into (abc) stationary frame as shown below.

$$\begin{pmatrix} i_{\alpha h} \\ i_{\beta h} \end{pmatrix} = \sqrt{\frac{2}{3}}\, inv\begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix}\begin{pmatrix} \tilde{i_d} \\ \tilde{i_q} \end{pmatrix} \tag{4}$$

Finally, the current from two phase stationary frame (αβ-0) is transformed back into three-phase stationary frame (abc) and the compensation reference currents i_a*, i_b* and i_c* are obtained us peer in (5).

$$\begin{pmatrix} i_a^* \\ i_b^* \\ i_c^* \end{pmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{pmatrix} i_{\alpha h} \\ i_{\beta h} \end{pmatrix} \tag{5}$$

Figure (3) illustrates the internal structure of SRF. The magnitude of peak reference current I_{max} which is the output of FLC is added to the extracted supply current DC component in (dq-0) reference frame. I_{max} takes response of the active power demand for harmonics and reactive power compensation.

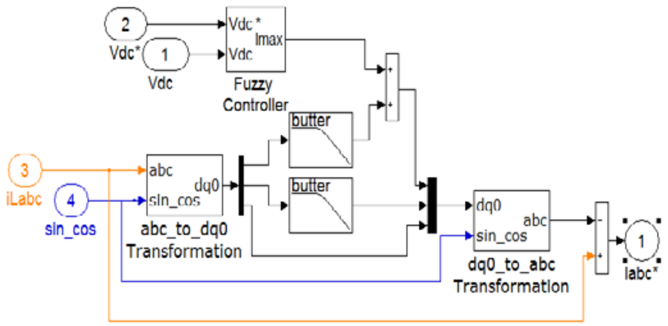


Fig. 3. Synchronous reference frame diagram

IV. TOPOLOGICAL OVERVIEW OF THREE LEVEL NPC INVERTER

Among the other multilevel topologies, 3L-NPC inverter has been widely used. The advantage is the lower current THD that reduces the filtering effort (less copper needed, lower losses in the filter). Using IGBTs and diodes with breakdown voltages (lower than the actual dc-link voltage) produce lower losses and the efficiency can be increased [15]. In Fig.4 a simplified circuit diagram of 3L-NPC inverter. Phase (A) consists of (04) semiconductors IGBTs (T1, T2, and T3&T4), (04) antiparallel Free-Wheeling Diodes (D1, D2, D3&D4), (02) Clamping Diodes (D5&D6).

The dc-link capacitors divide the DC bus voltage into three levels namely $-V_{dc}/2$, 0 and $V_{dc}/2$. These voltage levels appear at the output of each leg K (phase A, B or C) of the inverter by appropriate switching of the power semiconductor devices. The middle point of the two capacitors is denoted as ‘Z’ which is the neutral point [16].

Table.1 represents the switching states for phase (A) of a 3L-NPC .it can be obtained from (1)

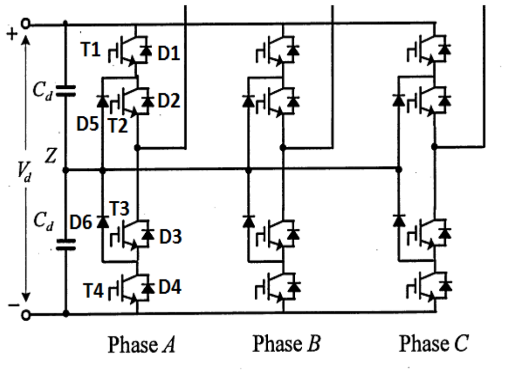


Fig. 4. Single leg of three level NPC inverter.

Switching states table of one leg of a 3L-NPC can be obtained from (6).

$$\begin{cases} T_{K3} = \overline{T_{K1}} \\ T_{K4} = \overline{T_{K2}} \end{cases} \qquad (6)$$

TABLE I
SWITCHING STATES FOR LEG (1) OF NPC 3-LEVEL

Output level Voltage	Switching States (k=1)			
	S1	S2	S3	S4
$\frac{V_{dc}}{2}$	1	1	0	0
0	0	1	1	0
$-\frac{V_{dc}}{2}$	0	0	1	1

V. HYSTERESIS CURRENT CONTROL

Hysteresis current control (HCC) is used for generating the switching pulses. It is the most extensively used technique because of the noncomplex implementation, outstanding stability, absence of any tracking error, very fast transient response, inherent limited maximum current, and intrinsic robustness to load parameters variations [17].

A. *Two-Level hysteresis current control*

Due to simplicity and quicker dynamic response, two-level HCC or fixed band HCC is one of the simplest and most robust current regulators available [18]. It operates by comparing a current error (the difference between measured and desired reference current) to create an instantaneous current error, and then compared against a fixed hysteresis band as per in Fig.5.

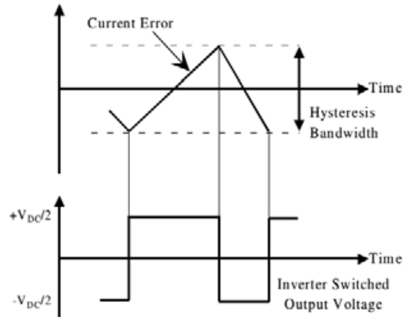


Fig. 5. Conventional two-level hysteresis current regulation

When the error falls below the lower hysteresis limit, the inverter phase leg output is switched high, and when the error rises above the upper hysteresis limit, the inverter output switches low. However, the main issue is its variable switching frequency which leads to extra switching losses and injecting high-frequency harmonics into the system current.

B. *Multilevel hysteresis current control*

For a multilevel inverter, when the current error exceeds a hysteresis boundary, the next higher (or lower) voltage level should be selected in order to ensure a single switch commutation to the new inverter state. For an N-level inverter, (N-1) bands are required with each band representing the switching between two adjacent voltage levels. Double band arrangement for controlling a 3L-NPC inverter is shown in Fig.6.

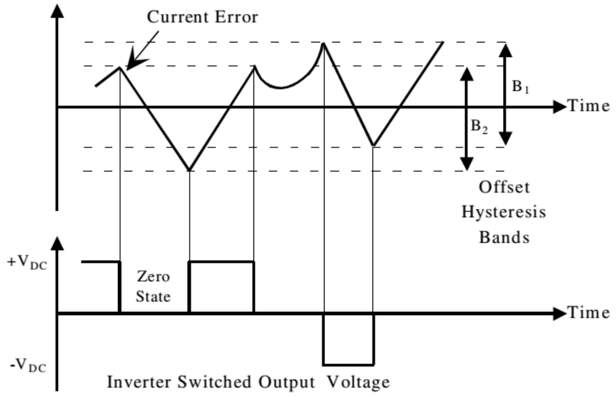


Fig. 6. Multi-band multi-level hysteresis current regulation

Author in [19] has given the double band HCC algorithm for 3L-NPC inverter us per in (7). where ΔI is the width of hysteresis tolerance band.

$$\begin{cases} \left.\begin{matrix}[(e_k \geq \Delta I)]\wedge[(e_k \leq 2\Delta I)] \\ \vee \\ [(e_k \leq -\Delta I)]\wedge[(e_k \geq -2\Delta I)]\end{matrix}\right\} \Rightarrow T_{k1} = 1 \wedge T_{k2} = 0 \\ [(e_k > 2\Delta I)\,] \Rightarrow \quad T_{k1} = 0 \wedge T_{k2} = 0 \\ [(e_k < -2\Delta I)] \Rightarrow \quad T_{k1} = 1 \wedge T_{k2} = 1 \end{cases} \tag{7}$$

And

$$\begin{cases} e_{k=(a,b,c)} = I_{k\_ref} - I_k \\ \begin{cases} I_{k\_upper} = I_{k\_ref} + \Delta I \\ I_{k\_lower} = I_{k\_ref} - \Delta I \end{cases} \end{cases} \tag{8}$$

The technique is robust but has the general limitation of requiring increasingly complex analog circuitry for implementing the multiple hysteresis bands and offset compensation as the number of voltage levels increases.

VI. DC BUS VOLTAGE REGULATION USING FUZZY LOGIC CONTROLLER (FLC)

A. Basic concepts of type-1 fuzzy sets

A type-1 fuzzy set in the universe X is characterized by a membership function $\mu_A(x)$ taking values on the interval [0, 1] and can be represented as a set of ordered pairs of an element and the membership value of the set. Its elements are defined in the following (9) and (10)

$$A = \{(x, \mu(x)), \mid \forall\, x \in X,\ \mu(x) \in [0, 1]\} \tag{9}$$

$$A = \int_{x \in X} \mu(x)/x \tag{10}$$

Where: ∫ denotes the collection of all points $x \in X$, with associated membership grade μ(x).

Type-1fuzzy set (T1 FS) is certain in the sense that its membership grades are crisp values witch minimize the effect of uncertainties.

As can be seen from Fig.7 a type-1 Trapezoidal, Triangular, and Gaussian membership functions (MF) μ(x), are constrained to be between 0 and 1 for all $x \in X$, and are two-dimensional functions. These types of MF do not contain any uncertainty, it means that exist a clear MF value for every input data point.

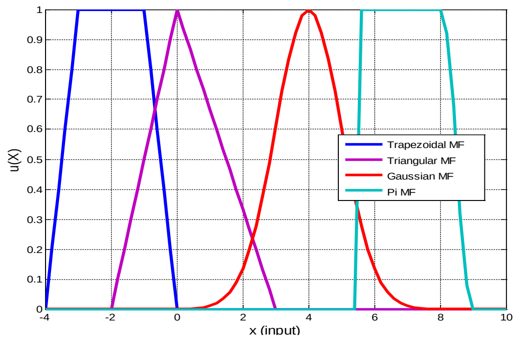


Fig. 7. Different categories of membership functions

The simplest MF is formed using straight lines. Of these MFs the simplest is the triangular; it is nothing more than a collection of three points forming a triangle. For basic structure of FLC, triangular category is chosen.

In general, a fuzzy logic system maps crisp input into crisp output and in such case contains three major modules:

1) Fuzzification

The fuzzification module converts the crisp values of the control inputs error signal and its variation into fuzzy values. A fuzzy variable has values which are defined by linguistic variables such as low, Medium, high, big, slow … where each is defined by a gradually varying membership function [20].

2) Fuzzy inference system and Knowledge base

$$R^l\!: If\ x_1 is\ A_1^l\ and\ x_2 is\ A_2^l\ and \ldots and\ x_p is\ A_p^l\ then\ y\ is\ B_p^l$$
$$x_1 \in X_1, \ldots, x_p \in X_p\ , l = 1 \ldots M \tag{11}$$

Where M is rule number, R^l is l^{th} rule, for p inputs and y is the output.

3) Defuzzification

Fuzzy logic controller output is converted from a linguistic variable to a numerical variable still using a membership functions.

B. Basic Structure of Fuzzy Logic Controller (FLC)

Mamdani fuzzy inference is based on the work of Lotfi Zadeh for complex systems and decision processes. This method is widely recommended as expert method for mastering fuzzy logic. The output from Mamdani FIS can be easily transformed to a linguistic form as the inference result before defuzzification [21].

Using Mamdani fuzzy model, the FLC is characterized us follows [22]:

- Seven triangular MF are used for error, variation error and δI_{max} as appear in Fig.8: NB (negative big), NM (negative medium), NS (negative small), ZE (zero), PS (positive small), PM (positive medium), and PB (positive big).

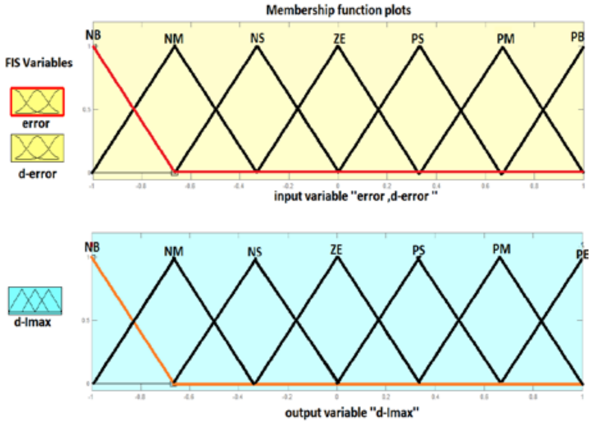


Fig. 8. Membership functions for e, Δe & δImax.

- Implication using 'min' operator
- De-fuzzification using the 'centroid' method
- Author considered (7x7) MF .While considering (3x3) or (5x5) MF, the shunt APF is unable to maintain the dc-link capacitor voltage constant and error voltage is developing due to voltage difference [23]. Based on this the rule table matrix are obtained as shown in Table2.

TABLE II
FUZZY RULE BASE MATRIX (7X7)

Δe e	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NS	NS	ZE	PS	PM
ZE	NB	NM	ZE	ZE	PS	PM	PB
PS	NM	NS	PS	PS	PM	PB	PB
PM	NS	ZE	PM	PM	PB	PB	PB
PB	ZE	PS	PB	PB	PB	PB	PB

In Fig.9 the internal structure of FLC is defined as (12).

$$\begin{cases} e(k) = V_{dc}^{*}(k) - V_{dc}(k) \\ \Delta e(k) = e(k) - e(k-1) \\ I_{max}(k) = I_{max}(k-1) + \delta I_{max}(k) \end{cases} \quad (12)$$

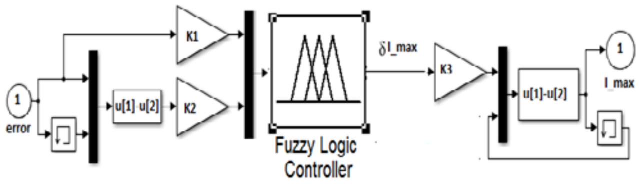


Fig. 9. Fuzzy logic corrector conception.

For better performance in the proposed controller, the processor parts of (K1, K2 and K3) are optimized in a specified range, after some trial and error, Author is able to find these values.

VII. SIMULATION AND DISCUSSING RESULTS

- This part presents the details of the simulation in Matlab/Simulink environment. Following table contains the system parameters considered for the study.

TABLE III
SYSTEM PARAMETERS

System	Parameters
Network	Vs=220V , F=50Hz
Nonlinear load	R_l=5Ω , L_l=8.10 $^{-3}$H
Shunt APF	C_f=2200.10 $^{-6}$F,L_f=1.10 $^{-3}$H
FLC	V_{dc}*=600V,(07)MFs,
HCC	ΔI=0.1A

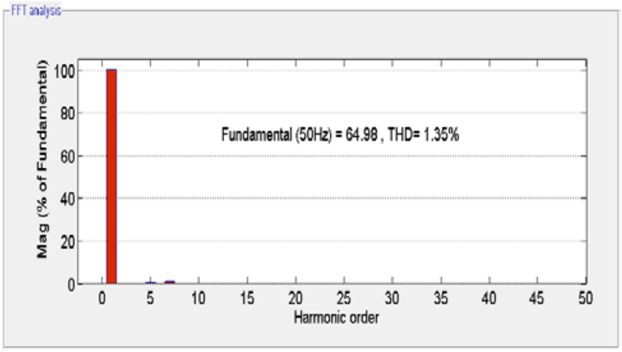


Fig. 10. Total harmonic distortion of source current phase (a).

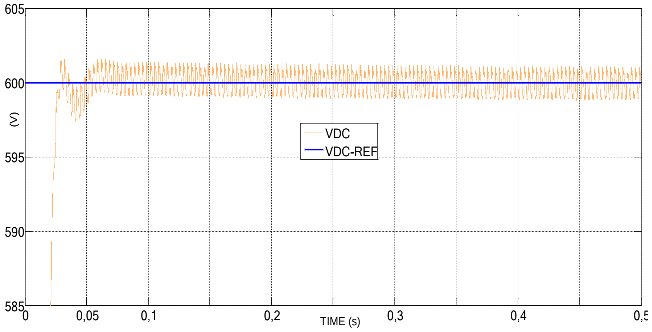
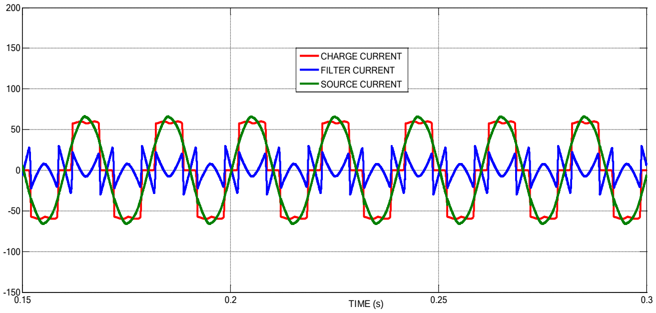


Fig. 11. Capacitor voltage and it reference.



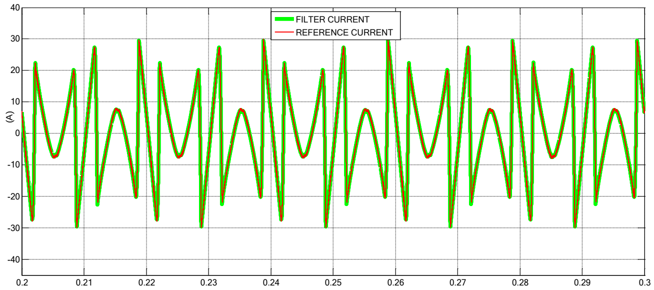


Fig. 12. Currents: source, filter and charge for phase (a).

Fig. 13. Current filter measured and its reference for phase (a).

The simulation results show a good filtering of harmonic currents and a perfect compensation of harmonics.

- The performance of the system has been practical remarked in Fig.10; the Total Harmonic Distortion value is less than 5%; harmonic limit imposed by the IEEE-519 standard.
- The filter capacitor voltage in Fig.11 has been maintained approximately at a constant value of 600V result explain the FLC controller performance.
- In Fig.12 Waveform of source current is purely sinusoidal after filtering using SRF approach.
- The HCC gives good performances and the measured current filter has been able to follow it reference by imposing the current band hysteresis observes in Fig.13.

VIII. CONCLUSIONS

In this research paper, our main objective being compensation of current harmonics generated due to the presence of non-linear load in three-phase three -level NPC shunt active power filter. Variable band hysteresis current regulation technique offers particular advantages; this is due to their very rapid dynamic response and robustness to load. This technique has the general limitation of requiring increasingly complex analog circuitry for implementing the multiple hysteresis bands and offset compensation as the number of voltage levels increases. Capacitor voltage regulation based FLC using different triangular fuzzy MFs provides good performance, however this controller suffers from non-linearity and uncertainty of developed system.

REFERENCES

[1] K. Frifita, M. Boussak, A. Naamane, N. M'Sirdi, "Improvement tolerant control of shunt active power filter under unbalanced Loads," IJ-STA, Vol. 10, N°1, Special Issue AND, pp 2079-2084, April (2016).

[2] E. Sundaram and M. Venugopal , "On design and implementation of three phase three level shunt active power filter for harmonic reduction using synchronous reference frame theory ," Electrical Power and Energy Systems,40–4,81(2016) http://dx.doi.org/10.1016/j.ijepes.2016.02.008

[3] A. K. Unnikrishnan, C. E. Sekaran, S.T. Joshi, A.S Manju and A. Joseph , " Shunt hybrid active power filter for harmonic mitigation: A practical design approach ," Indian Academy of Sciences ,Vol. 40, Part 4,pp.1257–1272, June (2015).

[4] S.R. Mohapatra,P.K. Ray ,G.H. Beng, "A partial feedback linearization based control design and simulation for three phase shunt active power filter," Measurement , 288-294,91(2016) http://dx.doi.org/10.1016/j.measurement.2016.05.075.

[5] K. Steela, and B. Singh Rajpurohit, "A survey on active power filters control strategies," 6th IEEE India International Conference on Power Electronics, pp. 1–6.Dec (2014).

[6] S. Rahmani, N. Mendalek, K. Al-Haddad , "Experimental design of a nonlinear control technique for three-phase shunt active power filter," Mathematics and Computers in Simulation, Sep(2015).http://dx.doi.org/10.1016/j.matcom.2015.09.007

[7] K. Benamrane, T. Benslimane, O. Abdelkhalek and T. Abdelkrim , "Control performance study of single stage three levels inverter output voltages for south Algeria PV system," J-STA, Vol. 9, N°1, pp 2035-2040, Dec (2015).

[8] F.L. Luo and H. Ye, "Multilevel DC/AC inverters," in Advanced DC/AC Inverters: Applications in Renewable Energy," 13: 978-1-4665-1138-5, by Taylor & Francis Group, LLC (2013).

[9] M. Frisch, "Advantages of NPC inverter topologies with power modules", [Online]. Available, (2011). http://www.neondrum.com.

[10] R. Belaidia, A. Haddouchea and H. Guendouz, "Fuzzy logic controller based three-phase shunt active power filter for compensating harmonics and reactive power under unbalanced mains voltages", Energy Procedia ,560-570,18(2012).

[11] V. Mahajan a, P. Agarwal and H.O. Gupta c, "An artificial intelligence based controller for multilevel harmonic filter", Electrical Power and Energy Systems, 170-180, 58 (2014).

[12] S. Mikkili, and A. K. Panda, "PI and Fuzzy Logic Controller based 3-phase 4-wire Shunt active filter for mitigation of current harmonics with Id-Iq control strategy,"Journal of power Electronics , vol. 11, No. 6, Nov(2011).

[13] L. Benyettou, T. Benslimane , K. Bentata and O. Abdelkhalek , "Open transistor faults characterization novel method for cascaded H-Bridge five-level three-phase shunt APF," AMSE JOURNALS Series: Modeling A; Vol. 88; N° 1; pp 53-70,(2015).

[14] K. Bhattcharjee, "Harmonic Mitigation by SRF Theory Based Active Power Filter using Adaptive Hysteresis Control," Power and Energy Systems: Towards Sustainable Energy, (2014).

[15] I. Staudt, "Note application," SEMIKRON: Innovation and service (2015).

[16] B.R. Lin and T.Y. Yang, " Three-level voltage-source inverter for shunt active filter ", Electric Power Applications, IEE Proceedings, vol. 151, no 6, pp. 744–751, Nov (2004).

[17] H. Vahedi,A. Sheikholeslami,M.T. Bina, and M. Vahedi, "Review ands of fixed and adaptive hysteresis current control considering switching losses and high-frequency harmonics", Advances in Power Electronics ,(2011), http://dx.doi.org/10.1155/2011/397872.

[18] S. Mikkili, and A.K. Panda, "Simulation and real-time implementation of shunt active filter Id–Iq control strategy for mitigation of harmonics with different Fuzzy membership functions," IET Power Electronics, Vol. 5, No. 9, pp.1856 – 1872, (2012).

[19] T. abdelkrim, B. el madjid, B. tarak and B. karima, "Feedback control of three-level PWM rectifier: Application to the stabilization of DC voltages of five-level NPC APF", Archives of Control Sciences 10.2478/v10170-010-0020-9, (2010).

[20] M. Blej and Mostafa Azizi , "Comparison of Mamdani-type and Sugeno-type fuzzy inference systems for fuzzy real time scheduling", International Journal of Applied Engineering Research, Vol. 11,pp. 11071-11075, 22 (2016).

[21] A. Kaur and K. Amrit, "Comparison of Mamdani-type and Sugeno-type fuzzy inference systems for air conditioning system", International Journal of Soft Computing and Engineering, Vol. 2, 2(2012).

[22] S.Kerrouch and F. Krim, "Three phase active power filter based on fuzzy logic controller", IJ-STA, Vol. 3, N°1, pp 942-955, Jul (2009).

[23] S. Mikkili and A. K. Panda, "Simulation and real-time implementation of shunt active filter Id–Iq control strategy for mitigation of harmonics with different Fuzzy membership functions," IET Power Electronics, Vol. 5, No. 9, pp.1856-1872, (2012).

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