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Modelling and Control of a Power Electronic Cascade for the Multi DC Bus Supply of a Three-Level NPC VSI

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Abstract. *Voltage source multilevel inverters have become very attractive for power industries in power electronics applications during last years. The main purposes that have led to the development of the studies about multilevel inverters are the generation of output voltage signals with low harmonic distortion; the reduction of switching frequency. A serious constraint in a multilevel inverter is the capacitor voltage–balancing problem. The stability problem of the input DC voltages in a Three-Level Neutral Point Clamping (NPC) Voltage Source Inverter (VSI) is recalled and illustrated in this paper. Power structure is proposed. It consists in using one CV rectifiers but the instability of intermediary DC voltages is observed. To solve this problem the power structure is modified by adding clamping bridges across capacitors in order to limit their deviations. The obtained results are full of promise to be used to stabilise the input DC voltages of this converter.*

keywords. *DSIM, Multilevel, NPC, VSI, Inverter, Clamping, Control, Modelling, Feedback.*

1. Introduction

The apparition of new power components controllable in the opened and closed states has let to the conception of new and fast converters for high power applications. Thus, drives have seen their cost decreasing considerably. The progress accomplished in the micro-computer tools has let the synthesis of more performing and robust control algorithms for machine drive.

High power applications in electrical traction require high voltage supply for motors. The only way to use multilevel converters is actually to generate voltages with high magnitudes [1], [2], [3]. These converters are built with a series connection of switches (Neutral Point Clamped Converters) or commutation cells (Flying Capacitor Converter) or full bridge converters (Cascaded multilevel converters). An additional advantage of multilevel converters is the Power Quality improvement of modulated voltages. Cheaper choke filters are then required. This paper deals with a Double Stator Induction Motors (DSIM) which is fed by a Three-Level NPC VSI. The critical problem of multilevel inverter is the deviation of capacitor voltages which are used in the multi DC bus for creating intermediary levels in modulated voltages. In the first part of this paper, we remind the model of the double stator induction motors [1], [2],[3]. Then, we elaborate the working model of this inverter, without presumption on its control [2], [3]. In the second part, we develop the space vector modulation strategy to control this inverter [2], [3]. In this part, the inverter is fed by constant input DC voltages. In the last part, we study the stability problem of the input DC voltages of the inverter. Thus, we study a cascade constituted by two three-level PWM rectifiers – two three-level NPC VSI – half clamping bridge – DSIM [3]. The results obtained show that the input DC voltages of the inverter are not stables. To improve the performances of the proposed cascade and stabilise the input DC voltages, the authors propose in this paper a solution which uses feedback for this cascade. The results obtained confirm the good performances of the proposed solution.

2. Model of the double stator induction machines

The model of the double stator induction machines (DSIM) is given by figure1.

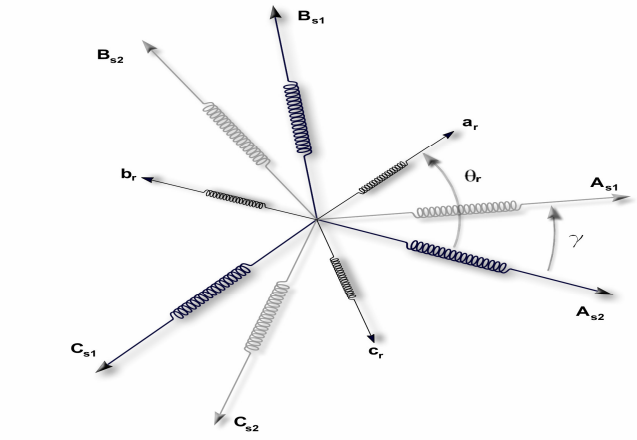

Fig.1. DSIM schema

Park model of the double stator induction machines, with P pairs of poles, is defined by the following equations system:

$$\begin{cases} V_{sd1}=r_{s1}i_{sd1}+\dfrac{d\varphi_{sd1}}{dt}-\omega\varphi_{sq1} \\ V_{sq1}=r_{s1}i_{sq1}+\dfrac{d\varphi_{sq1}}{dt}+\omega\varphi_{sd1} \\ V_{sd2}=r_{s2}i_{sd2}+\dfrac{d\varphi_{sd2}}{dt}-\omega\varphi_{sq2} \\ V_{sq2}=r_{s2}i_{sq2}+\dfrac{d\varphi_{sq2}}{dt}+\omega\varphi_{sd2} \\ V_{rd}=r_{r}i_{rd}+\dfrac{d\varphi_{rd}}{dt}-\omega_{gl}\varphi_{rq} \\ V_{rq}=r_{r}i_{rq}+\dfrac{d\varphi_{rq}}{dt}+\omega_{gl}\varphi_{rd} \end{cases}, \tag{1}$$

The electromagnetic torque is given by the following expression:

$$T_{em}=p\frac{L_m}{L_m+L_r}\left[\varphi_{rd}\left(i_{sq1}+i_{sq2}\right)-\varphi_{rq}\left(i_{sd1}+i_{sd2}\right)\right], \tag{2}$$

The model of the DSIM in the Park frame is given by figure2.

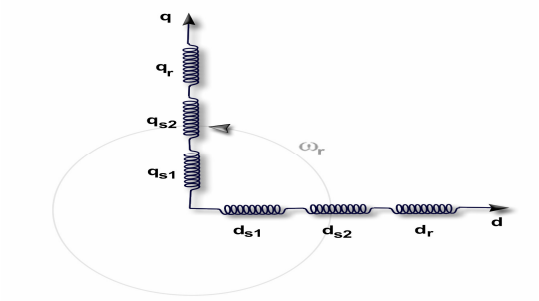

Fig.2. Representation of DSIM in the Park frame

3. Modelling and control of the three-Level NPCVSI

3.1. The three-level NPC VSI structure

The three phases three-level NPC VSI is constituted by three arms and two DC voltage sources. Every arm has four bi-directional switches in series and two diodes (Fig. 3) [3].

3.2. Knowledge model

The switch connection function F_{Ks} indicates the opened or closed state of the switch T_{DKs}.

We define too a half arm connection function F_{km}^{b} with:

k : arm number.

$$m = \begin{cases} 0 \text{ for the lower half arm} \\ 1 \text{ for the upper half arm} \end{cases}$$

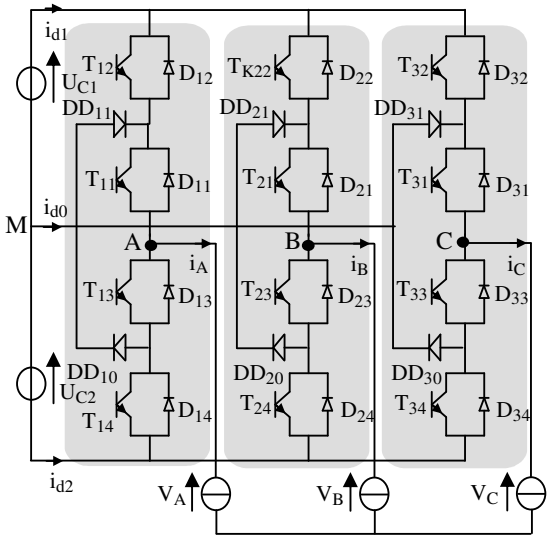

Fig.3. The three-level NPC inverter

For an arm k of the three-phase three-level NPC VSI, several complementary laws controls are possible. The control law which lets an optimal control of this inverter is [3]:

$$\begin{cases} B_{K4} = \overline{B}_{K1} \\ B_{K3} = \overline{B}_{K2} \end{cases}, \tag{3}$$

Where B_{Ks} represents the gate control of the switch T_{Ks}. We define the half arm connection function F_{i1}^{b} and F_{i0}^{b} associated respectively to the upper and lower half arms.

Where *i* is arm number ($i \in \{1, 2, 3\}$).

$$\begin{cases} F_{11}^{b} = F_{11}F_{12} \\ F_{10}^{b} = F_{13}F_{14} \end{cases}; \quad \begin{cases} F_{21}^{b} = F_{21}F_{22} \\ F_{20}^{b} = F_{23}F_{24} \end{cases}; \quad \begin{cases} F_{31}^{b} = F_{31}F_{32} \\ F_{30}^{b} = F_{33}F_{34} \end{cases}, \tag{4}$$

The output voltages of the inverter relatively to the middle point M are defined as follows:

$$\begin{bmatrix} V_{AM} \\ V_{BM} \\ V_{CM} \end{bmatrix} = \begin{bmatrix} F_{11}^b \\ F_{21}^b \\ F_{31}^b \end{bmatrix} U_{C1} - \begin{bmatrix} F_{10}^b \\ F_{20}^b \\ F_{30}^b \end{bmatrix} U_{C2}, \quad (5)$$

The system (5) shows that the three-level NPC VSI can be considered as two two-level voltage source inverters in series.

The input currents of the inverter are given as follow:

$$\begin{cases} i_{d1} = F_{11}^b i_1 + F_{21}^b i_2 + F_{31}^b i_3 \\ i_{d2} = F_{10}^b i_1 + F_{20}^b i_2 + F_{30}^b i_3 \end{cases}, \quad (6)$$

The current i_{d0} is defined by the following relation:

$$i_{d0} = (i_1 + i_2 + i_3) - (i_{d1} + i_{d2}), \quad (7)$$

3.3. PWM strategy of the three-level NPC VSI

The inverter is controlled by the space vector modulation strategy which uses two bipolar carriers.

This strategy is characterised by two parameters [2]:

- Modulation index m defined as ratio between the carrier frequency f_p and the reference voltage frequency: $\left[m = \frac{f_p}{f} \right]$.

- Modulation rate r is the ratio between the magnitude V_m of the reference voltage and three times of the carriers magnitude U_{pm}: $\left[r = \frac{V_m}{U_{pm}} \right]$.

The figure4 shows the signals of this strategy.

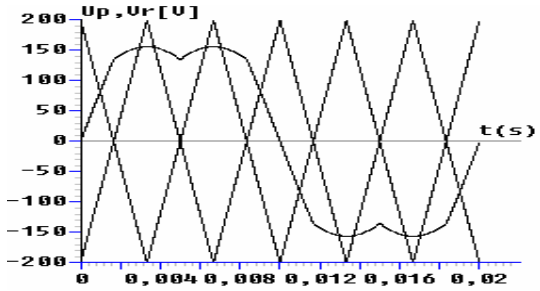

Fig.4. Space vector modulation strategy (m=6, r=0.8)

For even values of m, the output voltages present symmetry relatively to the quarter

of the period. Then, only odd harmonics exist. These harmonics gather by families centred around frequencies multiple of 2mf. The first family centred around frequency 2mf is the most important in view of its magnitude (Fig. 5).

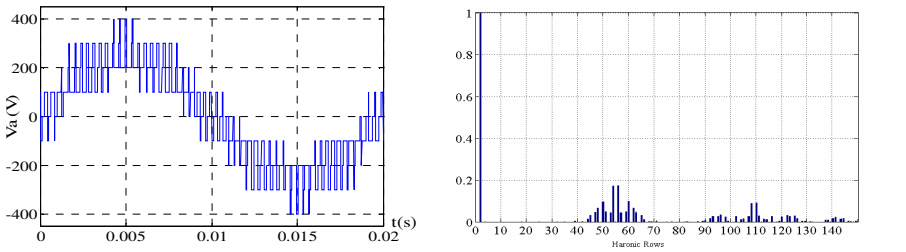

Fig.5. Simple voltage of the inverter and its spectrum (m=27)

4. Two three - level PWM rectifiers-filter – two three - level NPC VSI - DSIM cascade

Until now, we have supposed the input DC voltages of the three-level NPC VSI constants. In this part, we study a generation input DC voltages technique [3]. For this, we propose a cascade constituted by two three -level PWM rectifiers-filter-two three-level NPC VSI which feeds DSIM (Fig. 6). This cascade lets to absorb, in network, sinusoidal input currents with unity power factor.

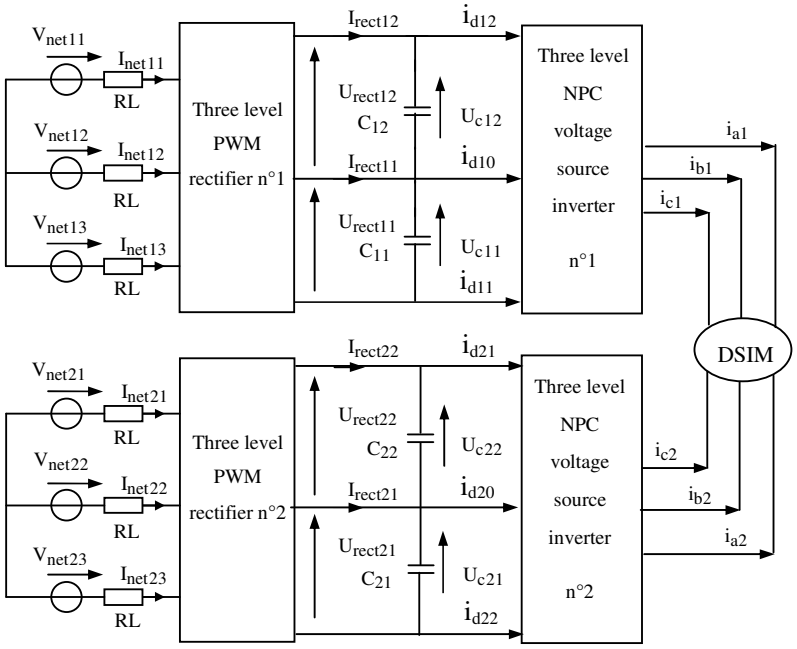

Fig.6. Two three-level PWM rectifiers-filter-two three-level NPC VSI-DSIM cascade

All

control strategies used for the two-level inverter can be used for the two-level PWM rectifier [3]. In this paper, they use the current hysteresis strategy to control this rectifier.

4.1. Modelling of the intermediate filter

The model of the intermediate filter is defined by the following system:

$$\begin{cases} C_{11}\dfrac{dU_{c11}}{dt} = I_{rect11} + i_{d11} \\ C_{12}\dfrac{dU_{c12}}{dt} = I_{rect12} - i_{d12} \\ C_{21}\dfrac{dU_{c21}}{dt} = I_{rect21} + i_{d22} \\ C_{22}\dfrac{dU_{c22}}{dt} = I_{rect22} - i_{d21} \end{cases}, \tag{8}$$

We note: $U_{rect1}=U_{rect11}+U_{rect12}$; and $U_{rect2}=U_{rect21}+U_{rect22}$.

4.2. Simulation results

The parameters of the intermediate filter are: $C_{11}=C_{12}=C_{21}=C_{22}$=10mf. The battery voltage is initialized at $U_{c11}=U_{c12}=U_{c21}=U_{c22}$=200V.

The different input voltages of the VSI are not stables and their differences are not null (Fig. 7). The output voltages of the two three-level rectifiers decrease continually (Fig. 8).

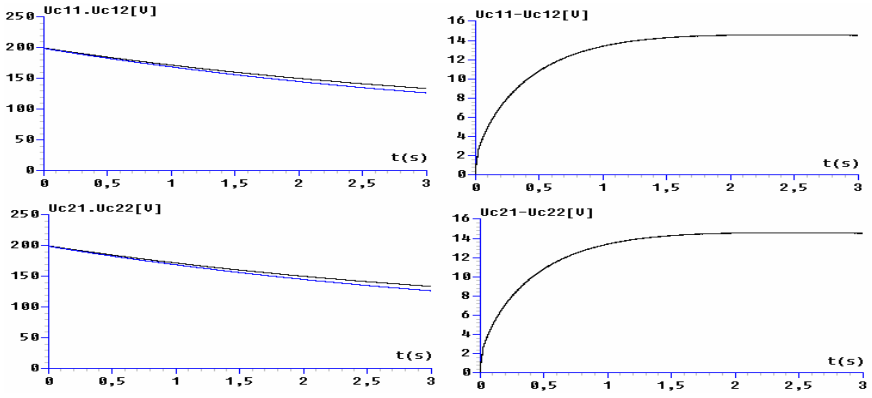

Fig.7. Input DC voltages of the two three-level NPC VSI

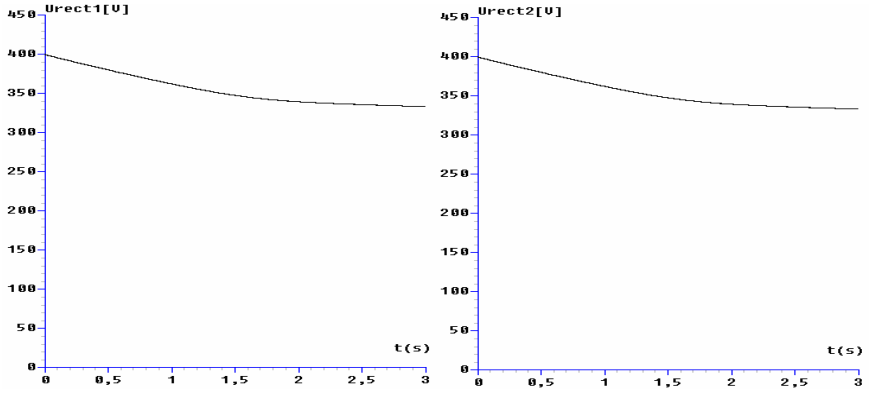

Fig.8. Input DC voltages of two the three-level NPC VSI

5. The half clamping bridge

To improve the input voltages of the three-level NPC inverter, we propose to use a half clamping bridge, constituted by a transistor and a resistor [3]. The transistors are controlled to maintain equal the different input DC voltages of the inverter (Fig. 9).

5.1. Modelling of the intermediate filter

Figure10 shows the structure of the intermediate filter of the studied cascade.

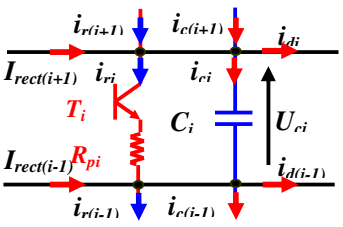

Fig.9. Clamping bridge cell

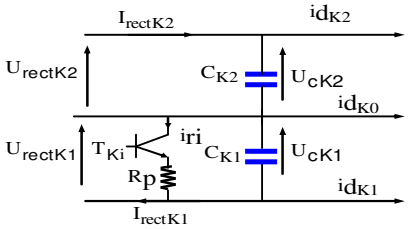

Fig.10. Structure of the intermediate filter of the of the half clamping bridge cascade

The model of the half clamping bridge-filter set is defined by the following equation:

$$\begin{cases} C_{K1}\dfrac{dU_{CK1}}{dt} = I_{rectK} - I_{dK1} - I_{ri}, \\ C_{K2}\dfrac{dU_{CK2}}{dt} = I_{rectK} - I_{dK2} \end{cases} \tag{9}$$

Where $$I_{ri} = \frac{U_{CK1}}{Rp}, \quad (10)$$

With:
i=1 for the first filter.
i=2 for the second filter.

The control algorithm of the resistive clamping circuits can be summarized as follows:

$$\text{If } U_{cK1} > U_{rectK1} \Rightarrow (T_{K1}=1) \,\&\, (T_{K2}=0)$$

5.2. Simulation results

We note that the input voltage of two three-level NPC VSI (U_{c11}, U_{c12}, U_{c21} and U_{c22}) become practically equals in bench regime and their differences are decreased to have a value practically null in steady state (Fig. 11). The output voltage of the two three-level are lightly increased (Fig. 12).

6. Three -level PWm rectifier feedback

In the previous part, we well-dressed obviousness the stability problem of the input DC voltages of the three-level NPC VSI. For resolve this problem, we propose the using the bridge clamping, because this bridge allow improve the input voltage of three-level inverter. In spite of this solution, the out put voltage of rectifier is not constant. For remedy of this problem, we propose the feedback of the input voltages of the three-level. The feedback low not only enslaves the input voltages of the inverter but as using a reasonable value of capacitors C_1 and C_2.

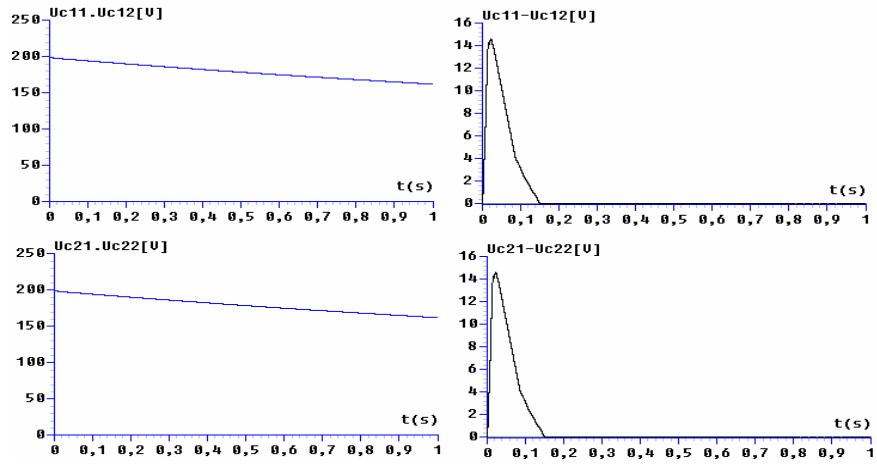

Fig.11. Clamping bridge voltage and their differences

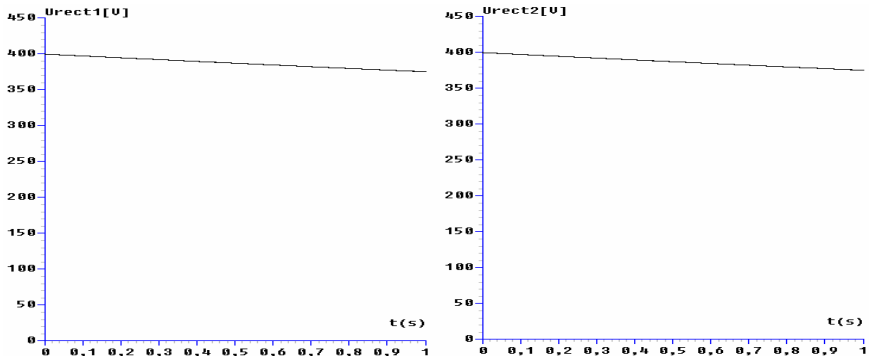

Fig.12. The input voltage of the clamping bridge

6.1. Voltage boucle model

The modelling of this boucle is based on principle of instantaneous power conservation with no loss hypothesis. This boucle imposes efficacy network reference current.

The input power is calculated as:

$$Pe = \sum_{k=1}^{3} (V_{netk}\, i_{netk} - Ri_{netk}^{2} - \frac{L}{2}\frac{di_{netk}^{2}}{dt}), \tag{11}$$

The output power is calculated as:

$$Pe = \sum_{i=1}^{2} (U_{recti}\, I_{recti}) = 2U_{rect}\, I_{rect}, \tag{12}$$

By neglecting Joule losses and assuming sinusoidal grid currents, we get:

$$3E_{eff}\, I_e = 2U_c I_{rect}, \tag{13}$$

Where E_{eff} is the rms value of grid voltages and I_e is the rms value of grid currents. U_c is the constant value of the DC capacitor voltage and I_{rect} is the DC current.
A IP regulator is used to regulate the DC voltage. The general principle feedback of three-level rectifier is shown on figure13.

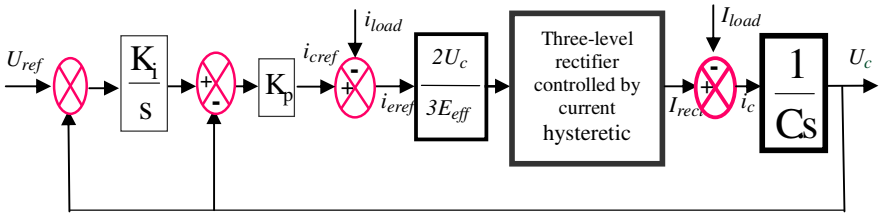

Fig.13. Enslavement algorithm of output voltage of three-level rectifier

6.2. Application of feedback algorithm of rectifier for the proposed cascade

We practice the feedback algorithm elaborate previously to control the rectifier of the cascade. The rectifier is controlled by the current hysteretic strategy

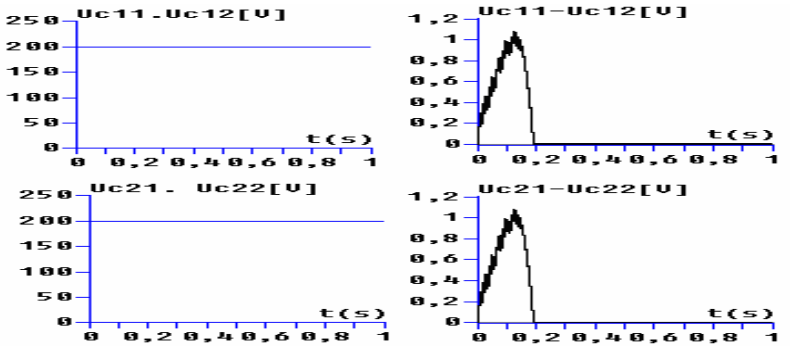

Fig.14. DC capacitor voltages

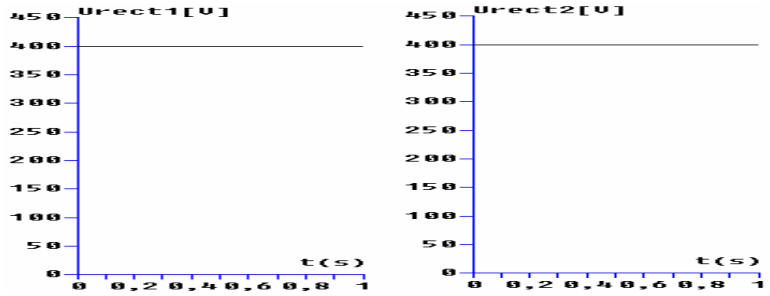

Fig.15. Output voltages of rectifiers

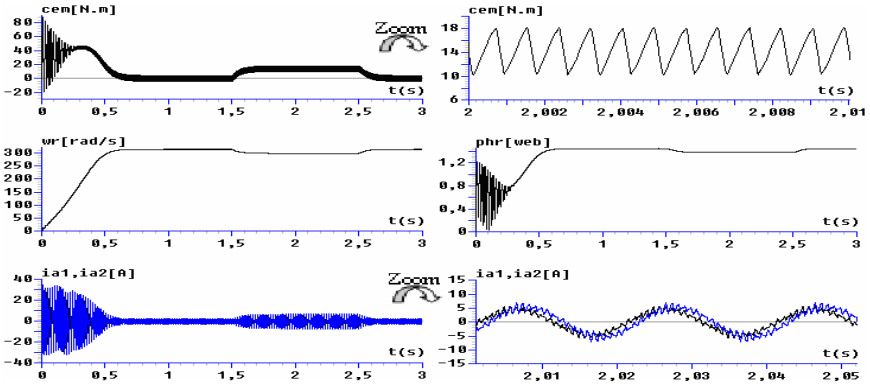

Fig.16. The DSIM performances

DC capacitor voltages are practically equal (Fig. 14). The controlled voltages of rectifiers are constant (Fig. 15). The performance of the speed control algorithm of the DSIM shows that the current of the machine nearly is sinusoidal. The speed and the torque effect for the charge variation between two instants t=1.5s and t=2.5s (Fig. 16).

7. Conclusion

In this paper we have proposed one power structure in order to stabilize intermediary DC voltages of a three-level NPC inverter. This power structure has been modelled and the control part has been explained.

The using of a half clamping bridge has allowed us to equalize the different input DC voltages of the inverter. In spite of this solution, the out put voltage of rectifier is not constant. For remedy of this problem, we propose to use the feedback algorithm of the output voltage of rectifier. The obtained simulated results show that the proposed solution is very efficient to solve the instability problem of the multilevel inverter.

References

1. D. Hadiouche, H. Razik, A. Rezzoug, "Study and simulation of space vector PWM control of double-star induction motors", IEEE-CIEP'2000, Acapulco, Mexico, pp. 42-47.
2. A. Monti, A. P. Morando, L. Resta, M. Riva, "Comparing two level GTO-inverter feeding a double-stator asynchronous motor with a three level GTO-inverter feeding a single star asynchronous motor", EPE'1995, Sevilla, Spain, pp. 2419-2425.
3. D. Beriber, M. Berkouk, A. Talha, M. O. Mahmoudi, "Study and Control of Two Two–Level PWM rectifiers–Clamping Bridge–Two Three Level NPC VSI Cascade. Application to Double Stator Induction Machine", IEEE 35th Power Electronics Specialists Conference, PESC'2004, Aachen, Germany 2004, pp. 3894-3899.