International Journal of Sciences and Techniques of Automatic control & computer engineering
IJ-STA, Volume 4, N° 1, July 2010, pp. 1126–1137.

Design and Performance Estimation of Delta Networks for MPSOC on Programmable Circuits

Yassine Aydi and Mohamed Abid

CES Laboratory, National Engineering School of Sfax, Tunisia
ENIS, Route de Soukra, Km 3.5-BP W, 3038 Sfax
E-mails: yassine.aydi@oous.rnu.tn, mohamed.abid@enis.rnu.tn

Abstract—Multiprocessor systems on chip (MPSoC) designs are increasingly being used in today's embedded system, to follow phenomenal increase of embedded products performance requirements. In these systems one of the most critical components regarding overall efficiency is on-chip interconnections which have a great impact on the performance constraints of modern MPSOC. Multistage interconnection networks have been frequently proposed as connection means in classical multiprocessor systems. They are generally accepted concepts in the semiconductor industry for solving the problems related to on-chip communications. This paper proposes the design and implementation of a flexible and scalable Delta network for MPSOC in an FPGA. The configurable Delta MIN provides a variety of network topologies with the convenience of a manager for configuration.

Keywords: NOC, MPSOC, DELTA MIN, FPGA

1. Introduction

Modern Multiprocessor system on chip (MPSOC) must satisfy many critical requirements: they have to be energy efficient, cheap, reliable, and must offer sufficient computing power for advanced and complex applications. To satisfy all these constraints simultaneously, future MPSOCs must integrate several types of processors and data memory units, adding more flexibility and programmability to these devices [1]. Therefore, researches were focused mainly in squeezing computing and controlling power on a system on chip (SoC). As a result, many MPSOC platforms have emerged [2].

A key step in the design of such systems is the choice of the communication architecture. Indeed, this communication architecture must support the entire inter-component data traffic and has a significant impact on the overall system performance [3]. As a promising alternative, Networks on Chip (NoCs) have been proposed by

This paper was recommended for publication in revised form by the editor Staff.
Edition: CPU of Tunis, Tunisia, ISSN: 1737-7749

academia and industry to handle communication needs for the future multiprocessor systems-on-chip [4]. In comparison with previous communication platforms (e.g., a single shared bus, a hierarchy of buses, dedicated point-to-point wires), NoCs provide enhanced performance and scalability. All NoCs advantages are achieved thanks to efficient sharing of wires and a high level of parallelism [5].

Multistage Interconnection Networks (MINs) have been used in classical multiprocessor systems. As an example, MINs are frequently used to connect the nodes of IBMSP [6] and CRAY Y-MP series [7]. Further on, MINs are applied for networks on chip to connect processors to memory modules in MPSOCs [8]. These architectures provide a maximum bandwidth to components (processors, DSP, IP...), and minimum delay access to memory modules. A MIN is defined by its topology, switching strategy, routing algorithm, scheduling mechanism, fault tolerance [9], and dynamic reconfigurability [10].

Performance evaluation is a key step in any MPSOCs design and especially of the selected communication architecture, allowing for decisions and trade-offs in view of system optimization. It is determined by modeling, using simulation [11], formal methods in which we use model checking and/or theorem proving techniques to verify instances of MINs [12] or direct execution which consists in the use of programmable logic circuits for fast performance evaluation [13].

A design and performance estimation of Delta MINs for MPSOC on an FPGA is investigated in this paper. Section 2 looks at some related work in this area. Next, MIN architecture is introduced. Section 4 describes in detail Delta networks model implemented on FPGA. Experimental results are detailed in section 5. Finally, we conclude the paper and we give directions for future work.

2. Related work

Applying the networking concept to on chip communication is the most important alternative for the design of modular and scalable interconnection platforms on chip to support growing computing requirements of future embedded applications. In the following, we briefly describe the different communication architecture designs proposed recently. We focalize on interconnection platforms implemented on FPGA.

Marescaux *et al.* [14] have proposed on interconnection networks which can be used as hardware components of an operating system managing reconfigurable systems on a chip. The platform is composed of three NoCs interfaced to reconfigurable IPs.

A design of an adaptable an FPGA-based Network on Chip dynamically reconfigurable has proposed by pionteck *et al.* [15]. By using dynamic routing tables, reconfiguration can be done without stopping or stalling the NoC.

Kumar *et al.* [16] have proposed a reconfigurable Multi Processor Network on Chip architecture in which both the network and the processing nodes are fully configurable, and the network is designed to match the application requirements.

Bobda and Ahmadinia [17] present two approaches addressing the problem of online reconfiguration of Network on Chip. First, they present a circuit-routing solution based on the concept of a reconfigurable multiple bus on chip (RMBoC). The second solution denoted a generic 2D dynamic model (DyNoC), targets devices with unlimited reconfiguration capabilities. The feasibility of the approaches has demonstrated through analysis and examples [17].

We proposed Delta multistage interconnection networks for MPSoC architecture on FPGA. To compare and contrast different MINs architectures, a standard set of performance metrics are evaluated.

3. MIN Architecture

In this section, we present an overview of the networks used for the design of the interconnection platform for MPSOCs on programmable circuits.

3.1 MIN Components

The common multistage interconnection networks (MINs) used, have N inputs and N outputs nodes and are built using $r \times r$ switches. Such MINs have N/r switches at each stage, and $log_r N$ stages of switches denoted d. The different stages are connected by links generated by applying permutation functions. Figure 1 represents a generic model of MINs of size $N \times N$ using crossbars with r equals 2.

In a MIN, a path between a source and a target is obtained by operating each corresponding switch of the stage i in straight mode if the i^{th} bit of the destination address is equal to 1, otherwise in exchange mode.

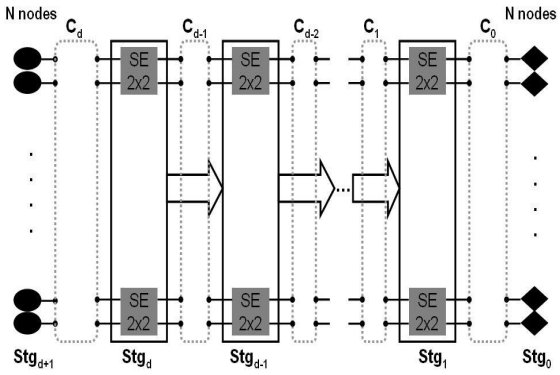

Figure 1. A generic model of MIN

3.2 MINs with Banyan property

We propose in figure 2 a topological classification of MINs. A banyan MIN is a multistage interconnection network characterized by one and only one path between each source and destination. A banyan MIN of size $N \times N$ consists of $r \times r$ crossbars. An interesting subclass of Banyan MINs is composed of Delta networks. Let denote by: o_i the i^{th} output of a crossbar in a MIN, and by C_j, a crossbar belonging to the stage j. So, the Delta property can be defined as follows: if an input of C_j is connected to the output o_i of C_{j-1}, then all other inputs of C_j must be connected to the stage $(j-1)$ on outputs with the same index i.

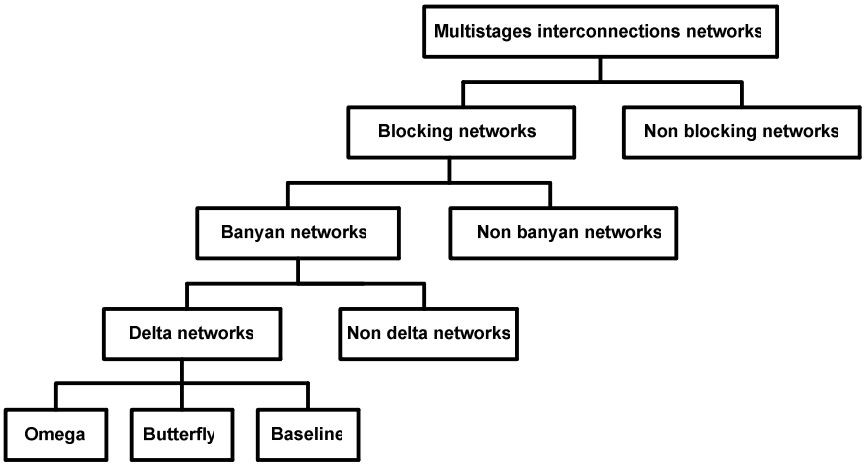

Figure 2. Classification of MINs

3.3 Delta networks

The difference between each of the existing MINs is the topology of interconnection links between the crossbar stages. A study of equivalence of a variety of Delta MINs (figure 3) has been detailed in [18].

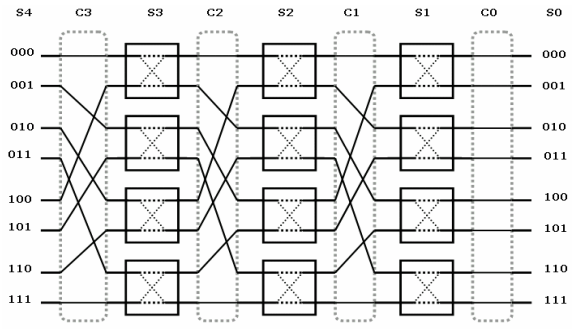

Figure 3. A Delta network (8,2)

We show in table 1 the links permutation of the most popular Delta MIN: omega, baseline and butterfly. Common links permutation used in a multistage interconnection network using 2x2 crossbar elements are:

- The perfect shuffle denoted **σ** is a bit-shuffling permutation where:

$\sigma^{k}(x_{n-1}\, x_{n-2} \ldots x_1 x_0) = x_{n-2} \ldots x_1 x_0\, x_{n-1}$.

- The butterfly permutation denoted **β** is a bit-shuffling permutation where:

$\beta_i^{k}(x_{n-1}.x_{i+1}\, x_i\, x_{i-1} \ldots x_1 x_0) = x_{n-1} \ldots x_{i+1}\, x_0\, x_{i-1} \ldots x_1 x_i$.

- The baseline permutation denoted **δ** is a bit-shuffling permutation where:

$\delta_i^{k}(x_{n-1} \ldots x_{i+1}\, x_i\, x_{i-1} \ldots x_1 x_0) = x_{n-1} x_{i+1}\, x_0\, x_i\, x_{i-1} \ldots x_1$

- The identity permutation denoted **I** is a bit-shuffling permutation where:

$\mathbf{I}(x_{n-1}\, x_{n-2} \ldots x_1 x_0) = x_{n-1}\, x_{n-2} \ldots x_1 x_0$

Links permutation	*stage (d+1)*	*stage k ∈ [1..d]*	*stage 0*
Omega	σ^{k}	σ^{k}	I
Baseline	I	$\delta_{(d-i)}^{k}$	I
Butterfly	σ^{k}	$\beta_{(d-i)}^{k}$	I

Table 1. Links permutation in Delta MINs

4. Proposed Model

In this section, we present the MINs architecture designed for Multiprocessor System on Chip platform. The model is fully implemented on an FPGA to suitably explore, evaluate and compare several NoC solutions with a very limited effort.

Additionally, the use of programmable logic circuits provides fast performance evaluation through emulation which is far superior to simulation.

4.1. The topology component

The configurable Delta MIN provides support for a variety of network topologies which play an important role in designing routing strategy, network latency, throughput and area. We will restrict study to Delta MINs networks (figure 3). That is the MIN has N inputs and N outputs nodes using a switches elements which have 2 inputs and 2 outputs ports. A generic connection block is developed to involve various MINs topology by switching links between the crossbar stages. This level of configurability performs flexibility for supporting different MPSOC application requirements.

4.2. Router architecture

The router is composed of 2x2 crossbars, a control component (arbiter), a couple of input and output ports (figure 4). Each input port of the router has dedicated buffer storage. Packets are buffered in input port until the output port of the next stage is ready to accept the packets; the width of each buffer is equal to the packet length in order to facilitate the routing strategy.

The packet format has two parts. The first part is the packet header that contains the source and target addresses and other bits for routing control. In The second part, we can store command, address, and data, in order to change traffic among processors and memories.

The connections between the ports change dynamically according the destination in the packet header. The round robin algorithm stored in the arbiter is activated when multiple inputs contain messages routed to the same output. The switching processes also occur in every stage in pipeline. To achieve the routing in MIN, we used the self routing algorithm. The path between source and target is obtained by operating each corresponding switch in stage i in straight mode if the i bits of the source and the target are equals, otherwise in exchange mode.

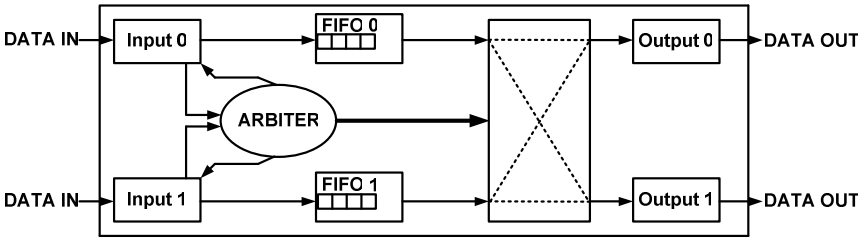

Figure 4. Router's architecture

4.3. Link manager

The goal is to have a communication infrastructure in which the reachability of packets is ensured, independent of the changing topology which occurs when connections are changed on the MPSOC. For enabling configuration in Delta MIN architecture, a link permutation manager is used to change the connections between stages. The following code describes the connections within the link manager.

```
architecture beh of manage is
begin
gen: for i in 0 to n/2 -1 generate
cs_out  (2*i)     <=  cs_in (i) ;
cs_out  (2*i+1)  <=  cs_in (n/2 + i) ;
addr (2*i)         <=   ram_adr (i) ;
addr  (2*i+1)     <=   ram_adr (n/2 + i) ;
data_in  (2*i)     <=  ram_data (i) ;
data_in (2*i+1)  <=  ram_data (n/2 + i) ;
write_en (2*i)     <=  ram_r_w (i) ;
write_en (2*i+1) <=  ram_r_w (n/2 + i) ;
end generate ;
end beh;
```

4.4. MINs implementation on FPGA

Generic model of a MIN for N processors and N memory have been implemented on a prototyping platform Altera Stratix II EP2S60. The following figure represents an example of an omega MIN (8, 2) described at RTL level.

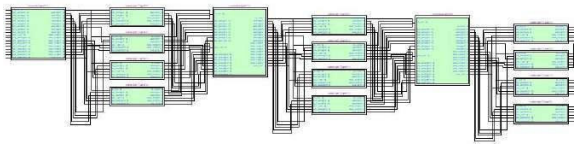

Figure 5. An Omega network (8,2)

The proposed MIN resource is detailed in the following table.

Resources		*Available*	*Used*	*%*
logical elements	*ALU*	48352	603	5%
	Logics register	48352	2017	
Memory blocks		2544192	49152	2%

Table 2. Resources of FPGA-Based MIN

Comparison of the synthesized model has been done against a full crossbar NOC (8x8) in order to evaluate area, energy consumption, and average latency. The following figure represents a full crossbar network (8,8) described at RTL level.

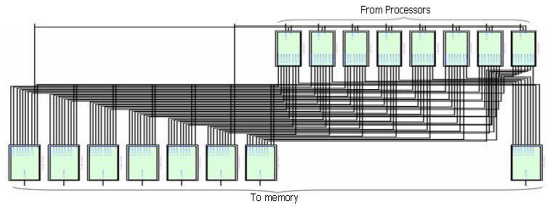

Figure 6 A full crossbar network (8,8)

4.5. Performance estimation of Networks

Our intention in this paper is to design and evaluate different topology of network through case studies of intensive data communication application with different number of cores. Subsequently, NOC evaluation metrics, such as area, energy consumption, and average latency became essential aspects for optimizing the implementation of network in MPSOC design.

A. Area evaluation

The proposed models of MIN consist of routers, links and connection blocks. Links connect cores to routers, and routers to connection blocks. Accordingly, the number of links resulted from any topology of MINs is the same. As a result, the number of links is not an important evaluation metric between different generation topology of MINS. Routers area is considered the main metric to evaluate the NoC area [19]. Moreover, input and output ports with their required buffering constitute the major percentage of any Crossbar area [20]. Beside routers that dominate the NoC area, and connection blocks constitutes another metric to evaluate the NoC area. Connection blocks perform various MINs topology by switching links between the crossbar stages.

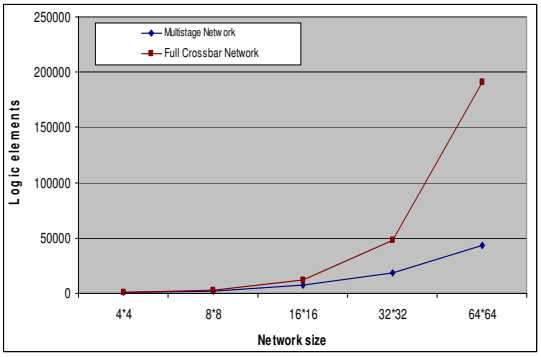

Figure 7. Percentage Area of Networks on FPGA

In the area evaluation, we compare a multistage interconnection network against a full crossbar network with different number of cores. Figure 7 shows the MIN area and the full crossbar area, respectively, resulted from simulation as the number of cores increases from 4 to 64. As the number of cores becomes large, we deduce that the percentage of MIN area settles at a low value, about 22%, compared to full crossbar network. These values confirm that the area of MIN is proportional to $N\log_2 N$; compared to N^2 for full crossbar network (N defines the number of processors).

B. Delay evaluation

Packet delay equals to the time taken by a packet to go through a network from its source to its intended target. Accordingly, in our delay evaluation, we define minimum and maximum delays respectively:

	minimum delay	*maximum delay*
MIN	$3 * \log_2 (N)) * T$	$(3 * \log_2 (N) + N-1) * T$
full Crossbar	$3 * T$	$(3 + N-1) * T$

Where N is the number of processors and T is the delay of packets through routers.

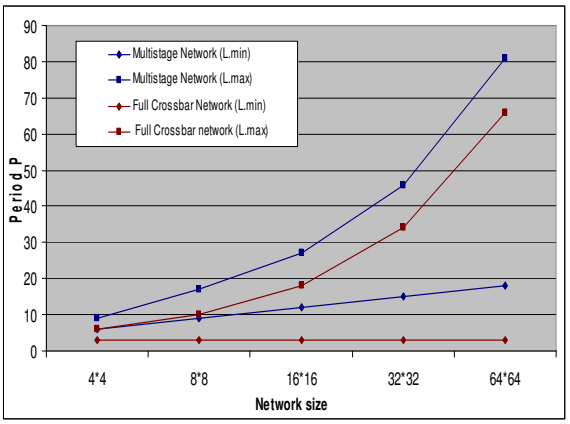

Figure 8. Packet delay Vs Node sizes

As shown in figure 8, the packet delays for the two networks are nearly 10 cycles when processor sizes equals to 4. Also, the minimum delay almost is constant for the full crossbar network, and it increases slightly for MIN network. Finally, we concluded that a full crossbar network is a little more efficient than the MIN network in terms of delay as the number of cores increases from 4 to 64.

C. Energy consumption

To evaluate the impact of the number of processors on the performance and the total consumption of the system, we use ALTERA Power Analyzer to measure the energy of a Delta MIN as the number of cores increases from 4 to 16. The following table reports the total energy consumption in mW.

	4*4 Nodes	8*8 Nodes	16*16 Nodes
Energy consumption	1591,78	1865,34	2065,74

Table 2. Energy consumption Vs node sizes

Given these results, it seems that adding processors to the system increases energy consumption. This can be explained as follow: it is evident when increasing nodes, the probability of conflict to occur in Crossbar increases and more waiting cycles dramatically alter overall performances, especially in terms of power consumption.

5. Test application

This section details the implementation of the configurable Delta MIN as well as complete MIN-based multiprocessor system. Our platform performs communication to N Mini-MIPS processors and N sharing data memories. The utility of the Delta MIN is shown here using a parallel matrix application. This algorithm is considered in important kernel in engineering applications. Generally, the asymptotic complexities of other algorithms depend directly on the complexity of matrix multiplication.

Table 3 presents the resource utilizations for 8*8 nodes implementation in the Altera Stratix II EP2S60. According these results, the averages of resource utilization for the proposed design are 53% of logical elements, 44% of DSP blocks and 21% of memory blocks.

	logical elements		*DSP blocks*	*Memory blocks*
	ALU	*Logics register*		
Processor	2.511	1.891	16	-
Delta MIN	603	2.017	-	49.152
Memory	-	-	-	131.072

Table 3. Resources utilization for 8*8 nodes

In order to demonstrate the effectiveness of the proposed design methodology, the selected application is parallelized on MPSoC architecture with 4 to 16 processors. Results are presented in figure 8.

The increase of processors to the system decreases execution time. This variation is not linear due to sharing resources. This requires waiting cycles and affects system

performance. In terms of area, it is significant that adding processors induces to consume more resources within FPGA.

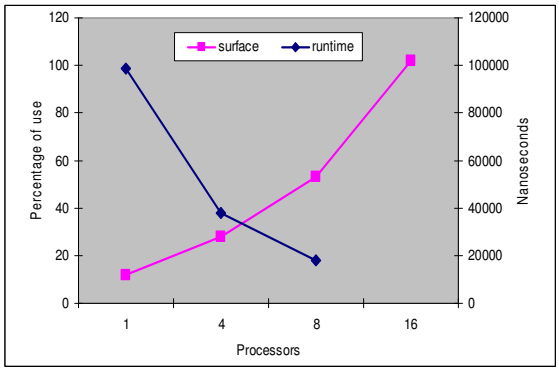

Figure 8. Execution time and area variation Vs processor sizes

6. Conclusion and future works

In this paper, we have proposed the design and the implementation of Delta multistage interconnection networks for MPSoC architecture in an FPGA. Our objective in this work is to provide a generic interconnection architecture for programmable circuit that can implement a variety of MIN based topologies in order to support different application requirements. To compare and contrast different MINs architectures, a standard set of performance metrics are evaluated, such as area, energy consumption, and latency. The synthesis results have detailed the resource utilization for complete MIN-based multiprocessor system.

Finally, later versions of Delta MIN platform will aim to support dynamic module replacement via partial reconfiguration. As mentioned, our platform provides support for configuring various topologies. We desire to investigate the use of this alternative in real applications where requirements change at run time and impose reconfiguring interconnection modules in an embedded system.

7. References

[1] A. Jerraya, and W. Wolf, "Multiprocessor Systems-on-Chips", Morgan Kaufmann Publishers, San Francisco, 2004.

[2] W. Wolf, "The future of multiprocessor systems-on-chips", Proc. of the 41st annual conference on Design automation, ACM Press, New York, 2004, pp. 681–685.

[3] S. Pasricha, "Floorplan-aware automated synthesis of bus-based communication architectures", Proc. of the 42nd annual conference on Design automation, ACM Press, New York, 2005, pp. 565–570.

[4] L. Benini, "Networks on chips: A new SoC paradigm", Computer, Vol. 35, N° 1, IEEE Computer Society Press, Los Alamitos, California, 2002, pp. 70–78.

[5] W. J. Dally, "Route packets, not wires: on-chip interconnection networks", Proc. of the 38th conference on Design automation, ACM Press, New York, USA, 2001, pp. 684–689.
[6] C. B. Stunkel, "The SP2 High-Performance Switch", IBM Systems Journal, Vol. 34, N° 2, IBM Corp., Riverton, USA, 1995, pp. 185–204.
[7] T. Cheung, "A simulation study of the CRAY X-MP memory system", IEEE Transactions on Computers, Vol. 35, N° 7, IEEE Computer Society, Washington, 1986, pp. 613–622.
[8] S.Duquennoy, "MpNOC Design: modeling and simulation", In 15th IP based SOC Design Conference (IP--SoC 2006), 2006.
[9] C.P. Kruskal, "The performance of multistage interconnection networks for multiprocessors", IEEE Transactions on Computers, Vol.32 , N° 12, IEEE Computer Society, Washington, 1983, pp. 1091–1098.
[10] Y. Aydi "Design and Performance Evaluation of a Reconfigurable Delta MIN for MPSOC", In 19th International Conference on Microelectronics (ICM '07), 2007.
[11] Y. Aydi, "Dynamicity Analysis of Delta MINs for MPSOC Architectures", STA'07, 2007.
[12] Borrione D., "A Formal approach to the verification of networks on chip", Eurasip Journal on Embedded Systems, , vol. 2009, 2009.
[13] Christophe Bobda., "Dynamic Interconnection of Reconfigurable Modules in FPGA", In IEEE Design & Test of Computers – Special Issue Networks on Chip. Vol. 2, No. 25, 2005, pp. 443-451.
[14] T.Marescaux, "Networks on Chip as Hardware Components of an OS for Reconfigurable Systems", In 13th International conference on Field Programmable Logic and Applications, 2003, pp. 595–605.
[15] T.Pionteck, "A Dynamically Reconfigurable Packet-Switched Network-on-Chip", in the conference on Design, Automation, and Test in Europe, 2006, pp. 136-137.
[16] A. Kumar, "An FPGA design flow for reconfigurable network-based multi-processor systems on chip", in the conference on Design, Automation, and Test in Europe, 2007, pp. 117–122.
[17] C. Bobda and A. Ahmadinia, "Dynamic Interconnection of Reconfigurable Modules on Reconfigurable Devices", IEEE Design & Test, Vol.22, N° 5, IEEE Computer Society Press, 2005, pp. 443–451.
[18] C. Kruskal, "A unified theory of interconnection network", Theoretical Computer Science, Vol.48, N°1, Elsevier Science Publishers Ltd., essex, 1986, pp. 75-94.
[19] W. Shen, "A new binomial mapping and optimization algorithm for reduced-complexity mesh-based on-chip network", in the IEEE International Symposium on Networks-on-Chip (NOCS'07), Princeton, 2007, pp. 317–322.
[20] M. Coenen, "A buffer-sizing algorithm for networks on chip using TDMA and credit-based end-to-end flow control", in the Third IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'06), Seoul, 2006, pp. 130–135.