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Five-Level Diode Clamped Active Power Filter for High Power Utilities

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Abstract. *Nonlinear loads have destructive effects in power systems. Active filters have been used as a solution to this problem. This paper presents the applications of five-level diode clamped Active Power Filter (APF) to the enhancement of medium voltage network power quality by compensation of harmonic currents produced by a nonlinear load. In the first part, the authors present a topology of five-level diode clamped Voltage Source Inverter (VSI), and its simplified Space Vector Pulse Width Modulation (SVPWM) control strategy. In the second part, to remedy to instability problem of the input DC voltages of this APF, the authors propose to use a clamping bridge filter. After that, the sliding mode regulator used to control the APF is developed. The simulation results confirm the suitable performance of the filter after balancing the DC bus and using the sliding mode regulator.*

Keywords. *Active Power Filter, Clamping bridge filter, Multilevel converter, Space Vector Pulse Width Modulation (SVPWM)*

1. Introduction

The wide use of nonlinear loads such as rectifiers, and cycloconverters has increased the harmonic and reactive power problems in AC lines [1]. These problems were partially solved in the past with the help of LC passive filters. However, this kind of filters cannot solve random variations in the load current waveform, produced by spikes or sudden amplitude variations. To solve these problems, shunt active power

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filters have been developed, which are today widely investigated. These filters work as a current sources, connected in parallel with the non-linear load, generating the harmonic currents the load requires. In this form the mains only needs to supply the fundamental, avoiding contamination problems along the transmission lines. Besides, with an appropriated control strategy, it is also possible to correct power factor and unbalanced loads.

Research on the shunt active filters implied different works concerning the harmonic identification methods such as Fourier transform method [2], the method of synchronous reference frame (d-q) [3], and control strategies such as sliding mode regulators, artificial neural networks and fuzzy logic controllers. The structure of the filters also knew an evolution, from two-level converters to multilevel converters. In high power applications, this latter is more adequate, compared to the conventional two-level structure, simply because of the low harmonic distortion rate of source voltage and current, low switching frequency besides no need to use transformer [4]. Various topologies are developed such as flying capacitor multilevel converters, diode clamped multilevel converters, NPC multilevel converters, and H bridge multilevel converters.

In this paper, first part is dedicated to the presentation of the model of the three phases five-level diode clamped VSI with its simplified SVPWM control method. In the second part, to remedy to instability problem of the input DC voltages of this APF, the authors propose to use a clamping bridge filter. This APF is applied for the enhancement of medium voltage network power quality by compensation of harmonic currents produced by a nonlinear load (Fig. 1). At the end the simulation results of sliding mode controlled APF are presented.

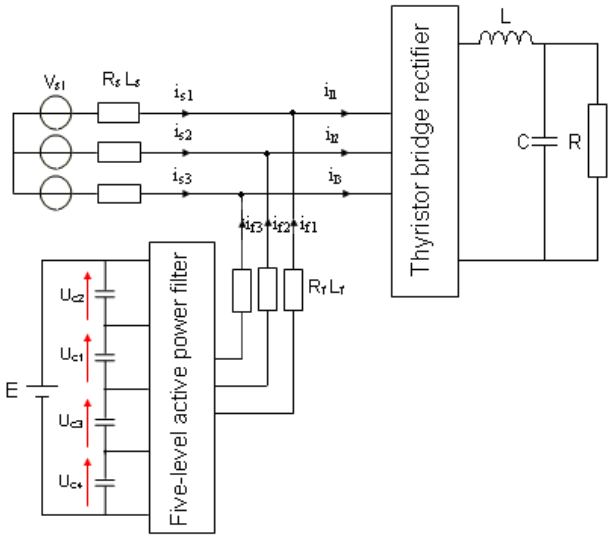

Fig. 1. Synoptic diagram of application of shunt APF on power supply fed a nonlinear load

2. Structure of five-level inverter

Structure of five-level diode clamped inverter is shown in Fig.2. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series dc-link capacitors split the dc-bus voltage in half. The necessary conditions for the switching states for the five-level inverter are that the dc-link capacitors should not be shorted, and the output current should be continuous [5].

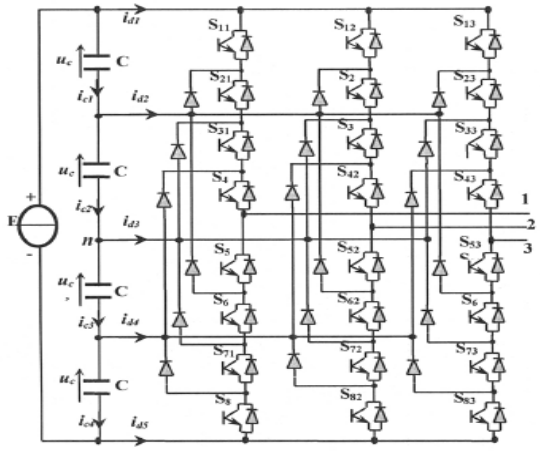

Fig. 2. Five-level diode clamped voltage source inverter

Each leg of the inverter has five possible switching states (Tab.1):

State P2: The upper switching devices S1x, S2x, S3x and S4x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = E/2.

State P1: The switching devices S2x, S3x, S4x and S5x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = E/4.

State 0: The switching devices S3x, S4x, S5x and S6x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = 0.

State N1: The switching devices S4x, S5x, S6x and S7x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = -E/4.

State N2: The lower switching devices S5x, S6x, S7x and S8x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = -E/2.

3. Inverter output voltages

For each switching device Sij (i = 1- 8, j = 1,2 or 3), we define a Boolean function Fij

as:

$$F_{ij} = \begin{cases} 1 & \text{if } S_{ij} \text{ is ON} \\ 0 & \text{if } S_{ij} \text{ is OFF} \end{cases} \tag{1}$$

The complementarities between upper and lower switching devices of each leg impose the following equations:

$$F_{ij} = 1 - F_{(i-4)j} \quad i = 5 \; to \; 8 \tag{2}$$

Table 1. States of five-level inverter

Switching Symbols	Switching States								Output Voltage
	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	S_{i7}	S_{i8}	
P2	ON	ON	ON	ON	OFF	OFF	OFF	OFF	E/2
P1	OFF	ON	ON	ON	ON	OFF	OFF	OFF	E/4
O	ON	OFF	ON	ON	ON	ON	OFF	OFF	0
N1	OFF	OFF	OFF	ON	ON	ON	ON	OFF	-E/4
N2	OFF	OFF	OFF	OFF	ON	ON	ON	ON	-E/2

For each leg of the inverter, we define five connection functions (one for each switching state) as:

$$\begin{cases} F_{c1j} = F_{1j}F_{2j}F_{3j}F_{4j} \\ F_{c2j} = F_{2j}F_{3j}F_{4j}F_{5j} \\ F_{c3j} = F_{3j}F_{4j}F_{5j}F_{6j} \quad j = 1,2 \; or \; 3 \\ F_{c4j} = F_{4j}F_{5j}F_{6j}F_{7j} \\ F_{c5j} = F_{5j}F_{6j}F_{7j}F_{8j} \end{cases} \tag{3}$$

The output phase voltages with reference to neutral point (n) of DC bus voltage are:

$$\begin{pmatrix} V_{1n} \\ V_{2n} \\ V_{3n} \end{pmatrix} = \begin{pmatrix} F_{c11} & F_{c21} & F_{c31} & F_{c41} & F_{c51} \\ F_{c12} & F_{c22} & F_{c32} & F_{c42} & F_{c52} \\ F_{c13} & F_{c23} & F_{c33} & F_{c43} & F_{c53} \end{pmatrix} \begin{pmatrix} E/2 \\ E/4 \\ 0 \\ -E/4 \\ -E/2 \end{pmatrix} \tag{4}$$

Fig. 3 shows the space vector diagram for five-level inverter.

Since five kinds of switching states exist in each leg, this converter has 125 switching states. The output voltage vector can take only 61 discrete positions in the diagram because some switches state are redundant and create the same space vector.

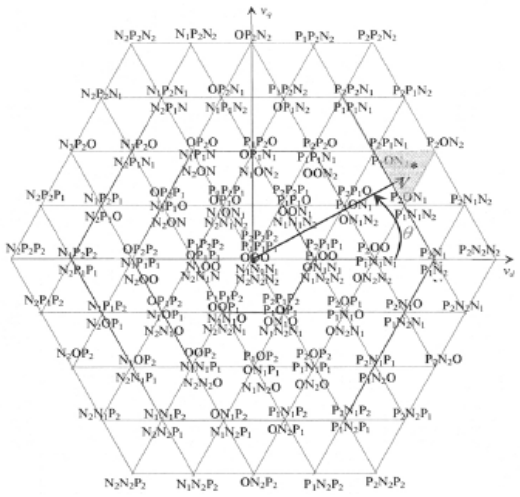

Fig. 3. Space vector diagram of a five-level inverter

4. SVPWM for five-level inverter

4. 1. Space vector modulation for two-level inverter

Fig. 4 shows the structure of two-level inverter. Each one of the three phases of the inverter has two switches and two freewheeling diodes. Depending on the values of the switching signals, the two-level inverter has eight states, summarized in table 2, where it is also indicated the output voltage vector produced in each state. These output vectors are shown on the space vector diagram of Fig. 5. It is also indicated an arbitrary reference vector V^*, to be generated by the inverter.

Table 2. States of two-level inverter

State	F_a	F_b	F_c	Voltage vector
0	0	0	0	V_0
1	0	0	1	V_1
2	0	1	0	V_2
3	0	1	1	V_3
4	1	0	0	V_4
5	1	0	1	V_5
6	1	1	0	V_6
7	1	1	1	V_7

The desired voltage vector, V^*, located in a given sector, can be generated by a linear combination of the two adjacent base vectors, v_x and v_y, which are framing the sector, and one of the two zero vectors v_z.

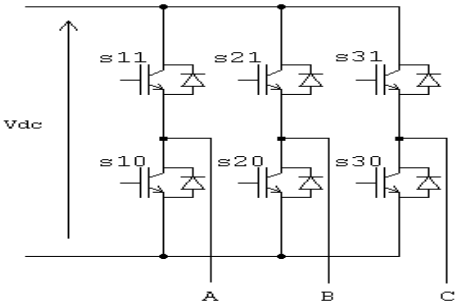

Fig. 4. Two-level inverter structure

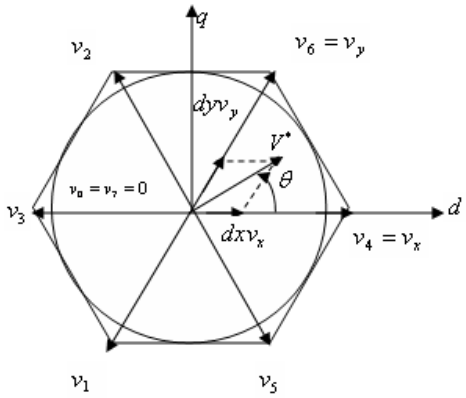

Fig. 5. Space vector diagram of two-level inverter

$$V^* = d_x v_x + d_y v_y + d_z v_z \tag{5}$$

d_x, d_y and d_z denotes the so called duty ratios of states X, Y and Z of the inverter within the switching interval, respectively. The duty ratios d_x, d_y and d_z are calculated as [6]:

$$\begin{aligned} d_x &= (|V^{2*}| / \sqrt{2/3}V_{dc})\ (\sin(60-\theta)/\sin(60)) \\ d_y &= (|V^{2*}| / \sqrt{2/3}V_{dc})\ (\sin(\theta)/\sin(60)) \\ d_z &= 1 - d_x - d_y \end{aligned} \tag{6}$$

4. 2. Simplified SVPWM for five-level inverter

The space vector diagram of a five-level inverter can be thought that is composed of six hexagons that are the space vector diagrams of the three-level inverters [7]. Each of these six hexagons, constituting the space vector diagram of a three-level inverter, centers on the six apexes of the medium hexagon as shown in Fig.6.

To simplify into the space vector diagram of a three-level inverter, two steps have to be taken. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the six hexagons. There exist some regions that are overlapped by two adjacent hexagons. These regions will be divided in equality between the two hexagons as shown in Fig. 7. Each hexagon is identified by a number S defined in equation (7).

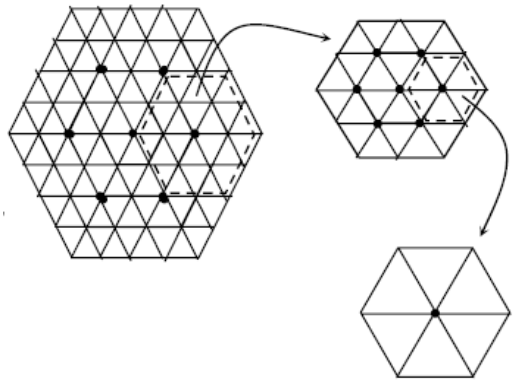

Fig. 6. Simplification of a five-level space vector diagram into two-level space vector diagram

Secondly, we translate the origin of the reference voltage vector towards the center of the selected hexagon as indicated in Fig. 8. This translation is done by subtracting the center vector of selected hexagon from the original reference vector. Table 3 gives the components d and q of the reference voltage V3* after translation, for all the six hexagons. The index (5) or (3) above the components indicate five or three-level cases respectively.

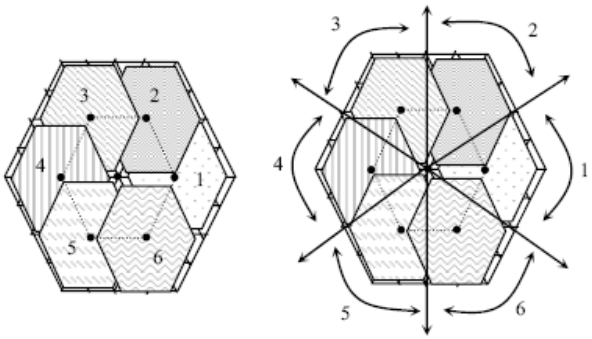

Fig. 7. Division of overlapped regions

$$s=\begin{cases}1 & if \quad -\pi/6<\theta<\pi/6\\ 2 & if \quad \pi/6<\theta<\pi/2\\ 3 & if \quad \pi/2<\theta<5\pi/6\\ 4 & if \quad 5\pi/6<\theta<7\pi/6\\ 5 & if \quad 7\pi/6<\theta<3\pi/2\\ 6 & if \quad 3\pi/2<\theta<11\pi/6\end{cases} \tag{7}$$

Table 3. Correction of five-level reference voltage vector

s	v_d^{3*}	v_q^{3*}
1	$v_d^{5*}-1/2$	v_q^{5*}
2	$v_d^{5*}-1/4$	$v_q^{5*}-\sqrt{3}/4$
3	$v_d^{5*}+1/4$	$v_q^{5*}-\sqrt{3}/4$
4	$v_d^{5*}+1/2$	v_q^{5*}
5	$v_d^{5*}+1/4$	$v_q^{5*}+\sqrt{3}/4$
6	$v_d^{5*}-1/4$	$v_q^{5*}+\sqrt{3}/4$

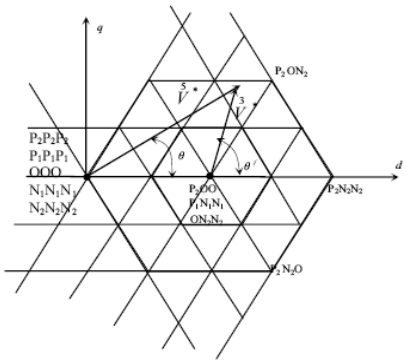

Fig. 8. Translation of five-level reference voltage vector

To simplify into the space vector diagram of a two level inverter, we have to take the two steps mentioned above. Fig. 9 shows the translation of three-level reference voltage vector. The correction of its reference voltage vector is presented in table 4.

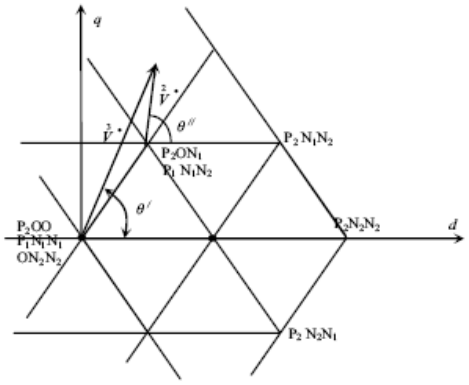

Fig. 9. Translation of three-level reference voltage vector

Table 4. Correction of three-level reference voltage vector

s	v_d^{2*}	v_q^{2*}
1	$v_d^{3*} - 1/4$	v_q^{3*}
2	$v_d^{3*} - 1/8$	$v_q^{3*} - \sqrt{3}/8$
3	$v_d^{3*} + 1/8$	$v_q^{3*} - \sqrt{3}/8$
4	$v_d^{3*} + 1/4$	v_q^{3*}
5	$v_d^{3*} + 1/8$	$v_q^{3*} + \sqrt{3}/8$
6	$v_d^{3*} - 1/8$	$v_q^{3*} + \sqrt{3}/8$

5. Modeling and control of clamping bridge

The clamping bridge cell is a simple circuit constituted by a transistor and a resistor in series connected in parallel with a capacitor as shown in Fig. 10. The transistors are controlled in order to maintain the equality of the different voltages [8].

In this part, the model of this filter with clamping bridge is defined by the following equation:

$$C_i(dU_{ci}/dt) = Ired_i + ir_{(i+1)} + ic_{(i+1)} - id_i - ir_i \tag{8}$$

with: $ir_i = T_i(U_{ci}/R_i)$

The transistor is controlled using the following algorithm:

$$\begin{cases} \varepsilon_i = U_{ci} - U_{cref} \\ \text{if } \varepsilon_i > dr \text{ on a } T_i = 1 \Rightarrow ir_i = T_i(U_{ci}/R_i) \\ \text{if } \varepsilon_i < -dr \text{ on a } T_i = 0 \Rightarrow ir_i = 0 \end{cases} \tag{9}$$

dr : hysteresis band width.

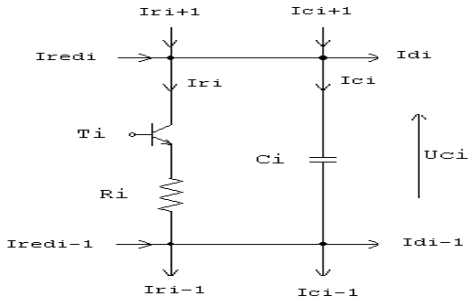

Fig. 10. Clamping bridge cell

6. Active power filter control

Active power filter is controlled using sliding mode regulator [9],[10]. From the model of active filter associated to supply network (10) and by considering the error between harmonic current reference and the active filter current as sliding surface (11), and the smooth continuous function as attractive control function (12), one gets the control law (13).

$$V_{frefK} - V_K = R_f i_{fK} + L_f (di_{fK} / dt) \tag{10}$$

with: $V_K = V_{sK} - R_s i_{SK} - L_s (di_{sK} / dt)$; K = 1,2 and 3

$$S_s = i_{frefK} - i_{fK} \tag{11}$$

$$U_n = k.(S_s / (|S_s| + \lambda)) \tag{12}$$

$$V_{frefK} = R_f i_{fK} + L_f (di_{frefK} / dt) + V_K + k(S_s / (|S_s| + \lambda)) \tag{13}$$

7. Simulation results

A medium voltage source of 5.5kV, 50Hz feeds a nonlinear load as illustrated in Fig. 1. This load produces a distorted current of 62 % THD which is above the tolerated THD limit standard. This current with its spectral analysis are presented in Fig. 11.

Fig. 12 shows DC bus capacitors voltages of APF before and after application of clamping bridges. Before t=2s, these voltages are unbalance. Application of clamping bridges allows getting stable capacitors voltages around there reference of 3kV.

Reference identified harmonic current ifref1 and output filter current if1 are almost identical as presented in Fig. 13.

Fig. 14.a presents main source voltage Vs1 and current is1 after harmonic current compensation. Spectral analysis is presented in Fig. 14.b. It is shown that source current is almost sinusoidal with THD less than 5% and unity power factor.

Simulation Parameters:
Main source:
V(ph-ph) = 5.5k V, f = 50 Hz, Rs = 0.0001Ω, Ls = 0.001H.
Load:
L = 0.005H, R = 20 Ω, C = 0.01F .
Active power filter:
Rf = 0.0001 Ω, Lf = 0.0025 H, C = 0.05 F, fc =3 kHz.

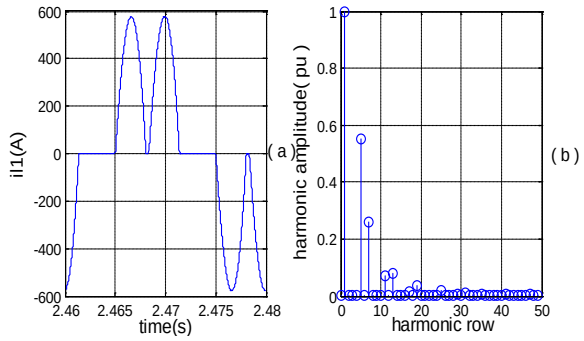

Fig. 11. Current drawn by the nonlinear load THD = 62%

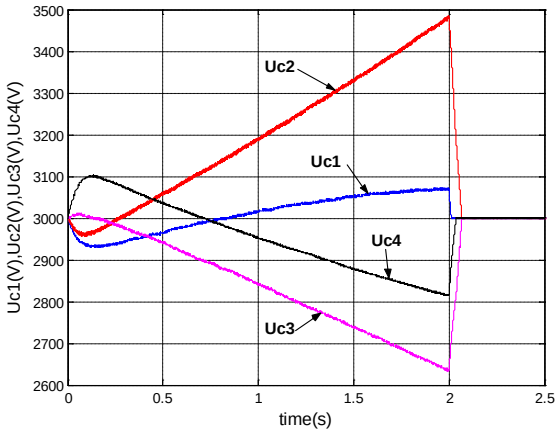

Fig. 12. DC bus capacitors voltages of five-level APF

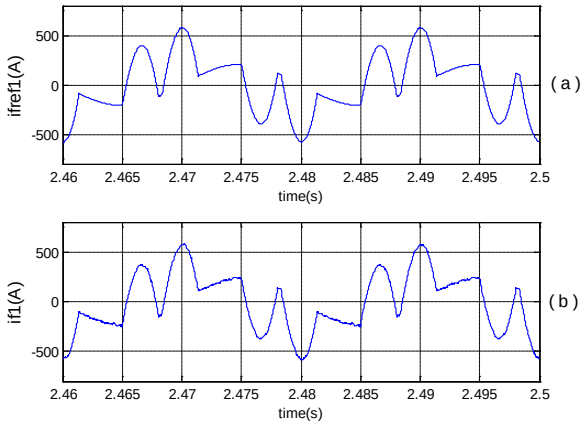

Fig. 13. Reference harmonic current ifref1 and filter output current if1

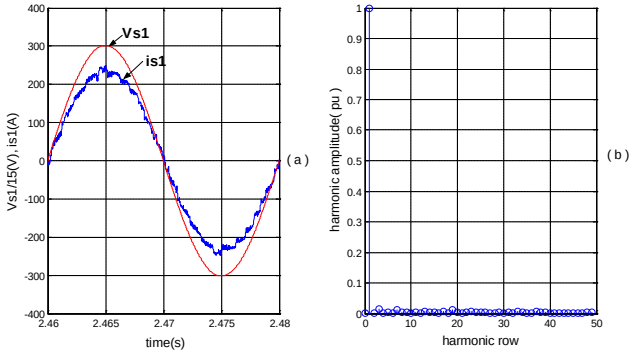

Fig. 14. Main source voltage Vs1and current is1 with its spectral analysis (THD=3.2%)

8. Conclusion

This paper presents a simplified SVPWM associate with sliding mode regulator for a diode clamped multilevel converter with equal input DC sources. The model and the simplified SVPWM of this power converter have been developed. After that, a clamping bridge filters has been introduced to solve the instability problem of the DC sources. A simulated system of a shunt APF based on five-level diode clamped converter is established. Simulated results verify that this APF can compensate the har-

monic currents and reactive power correctly and validly, which has perfect prospect in engineering application.

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